Abstract

VIJAYARAGHAVAN, RAVI COMMANDUR. Substrate Noise Analysis in RF Integrated Circuits. (Under the direction of Dr. Michael B. Steer and Dr. Antonio Montalvo.)

Substrate coupling in integrated circuits is the process whereby, parasitic current flow in the substrate, electrically couples devices in different parts of the circuit. Higher levels of integration and higher frequencies of operation makes the coupling more pronounced in modern circuit realizations. Electrical coupling in the substrate leads to undesirable interaction between devices which can degrade circuit performance. The degradation can manifest itself in different ways. In mixed analog-digital circuits, for example, the switching-noise generated by digital circuits can be coupled to sensitive analog circuits through the substrate.

Performance degradation due to substrate coupling can be addressed at the circuit design stage by including substrate models in circuit analysis. Analytical models based on simple substrate resistance plots are developed. Trends in substrate resistance variation for different substrates are studied to understand its effect at the circuit level. Analytical model for measurement of substrate coupling at the circuit level based on substrate resistance information and other circuit parameters is developed. Efficient techniques to improve isolation based on simulation and analysis of the substrate model are discussed.

Substrate Noise Analysis in RF Integrated Circuits

by

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Biographical Summary

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I fail to find words to express my deepest sense of gratitude to my Father and Mother for being the source of all the good thing i have earned in Life till date. I thank my sister for being a source of inspiration. They are God's greatest gift to me in Life. Heartfelt thanks to my friends for their encouragement.

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Chapter 1

Introduction

1.1 Motivation

The growth of the personal communications market has led to a great demand for low-power radio-frequency circuits with high levels of integration for portability and compact sizes. Increased device density, feature minimization, chip size, as well as overall higher frequencies of operation, have made problems of substrate noise critical in the design of integrated circuits. In single chip solutions, integrating noise-generating circuits and low-noise circuits on the same substrate is still viewed as a major challenge by circuit designers.

Higher levels of integration have several associated advantages and disadvantages. An obvious advantage is the reduced package count. This leads to lowered costs and reduced sizes.The power dissipation can also be reduced as fewer pads and interconnect lines need to be driven, thereby avoiding the associated capacitance. Indirectly, this may improve the high frequency response of circuits or even extend the frequency range of circuit performance, as the package interconnect parasitics often degrade the frequency response at the high-frequency end of the application.

A major disadvantage of integration is the increased interaction between circuits. This interaction can appear in two major ways. One can be through the significant mutual inductances and capacitances that exist between any two bond wires and pins in the package. The second significant mode of interaction is through the common

substrate shared by the circuits in the chip. Currents can flow through the substrate due to the nonzero dielectric constants and conductivities of the substrate material and couple circuits located in different parts of the circuit.

Substrate noise analysis in different substrate type is analyzed in this thesis. Noise coupling in different circuit topologies is studied and techniques to improve isolation using circuit techniques in different circuit topologies is studied and verified.

1.2 Thesis Outline

The outline of the thesis is as follows.

Chapter 2 gives a brief literature review on available papers on substrate noise analysis specific to the problem of noise coupling in various topologies including softwares developed.

Chapter 3 discusses the common sources of coupling in circuits with information on how substrate noise is injected, transmitted and received through them.

Chapter 4 presents a detailed analysis of the substrate resistance model for two different substrates along with analytical model to measure coupling and predict isolation. Circuit design techniques to improve isolation for different substrate type is studied based on the analysis for different circuit topologies.

Chapter 5 gives a conclusion for the analysis done in chapter 4 along with directions for future research in this area.

Chapter 2

Literature Review

2.1 Introduction

Substrate noise analysis has been a topic of research for the past few years in various levels of IC design. With increasing levels of integration, increasing density in packaging of circuits, reduction in feature size and package size the issue of substrate noise coupling is growing. Research have been done at various levels to understand substrate noise issues in Integrated Circuits(ICs). Papers and literatures have been published in the recent past on issues of modeling substrate noise, techniques to substrate noise optimization. Also softwares, commercial and non-commercial, based on various modeling techniques for circuit analysis have been developed. The software developed have been used to determine effectively compute resistance matrix for circuit simulation with substrate information. Also substrate analysis specific to certain RF applications have also been studied and recorded in the industry and academia. This section gives a brief review of some available papers, literatures and softwares on substrate analysis.

2.2 Review of Available Papers

Analysis and Modeling of substrate coupling in ICs were addressed in Reference [1]. This paper discusses a numerical technique to model the substrate for faster analysis of substrate impedance matrix for circuit analysis of the substrate. The technique presented in the paper utilizes the substrate Green's function to generate the impedance matrix between contacts, where contacts are defined as the device-to-substrate junctions. The inverse of the impedance matrix provides the admittance matrix which is included in a circuit simulator to determine the effects of coupling through the substrate. As explained in the paper, the admittance matrix aids in faster matrix computation using the Fast Fourier Transform technique. This reduces the computation complexity and lesser computation time. The results provided in this paper, and related material to this paper from the same author, provide theoretical information on substrate analysis and also simulation results for various substrate based circuits. The results from of this paper are compared with the simulation results carried out in this thesis using a commercially available EM tool.

The technique of substrate extraction to generate circuit model for analysis was also discussed in [2]. The author talks about a new technique based on the Boundary Element Method of numerical analysis based on a suitable choice of Green's function. This technique avoids numerical analysis of potentials and currents in a substrate based on finite element method which is more computationally expensive to be used in standard CAD system. This technique hence adopts the technique to avoid a full characterization of the complete substrate and allows a straight forward computation of a fully specific equivalent electrical network. The circuit model thus formed can be merged with the original circuit to analyze the effects of cross-talk in the circuit. The method described in this paper has been fully implemented in many layout-to-circuit simulators. The author and his group has implemented a similar layout-to-circuit simulator for substrate resistance modeling called *SPACE*. The downloadable version of the software with other related publications is available in [3]. Recent publications by the same group talks about the use of both Finite Element Method and Boundary Element Method in conjunction with one another to improve the performance of

their in-house substrate resistance modeling software, *SPACE*, for accurate and faster execution time of the application.

Results of substrate analysis and modeling done during the same period as the earlier two papers discussed, was provided in [4]. The author discusses several approaches used for accurate simulation of substrate coupling. One approach has been to first generate a 3D RC mesh using spatial discretization of Maxwell's equations on the substrate and then to reduce the resulting large network of passive elements into a small $n \times n$ macromodel of admittance parameters where n is the number of ports (devices, contacts) connected to the mesh. He also discusses the macromodeling/ network reduction using the Asymptotic Waveform Evaluation Technique. In all these researches, the substrate is considered purely resistive as the effects of parasitic substrate capacitance is not seen at operating frequencies of say up to 10 GHz. With this assumption the 3D resistive mesh is reduced to a set of $n(n+1)/2$ resistance interconnecting n ports using a simple dc macromodeling approach. Also the alternative approach using the Boundary Element Technique of modeling the substrate is discussed where the modified Green's function is used to model the substrate resistance. The author also talks about incorporating the combination of both techniques in a extraction tool for substrate parasitics *SUBTRACT* in [5].

Till now, there have been a few publications and related links to information on efficient modeling of substrate parasitics. In [6] and [7] the authors talk about substrate optimization techniques based on semi-analytical techniques to be used in physical optimization tools. They talk about techniques to fast and accurate estimation of the impact of technology migration and/or layout redesign on substrate noise and, ultimately, on the circuit's overall performance. The suitability, of the approach is shown through tests on industrial-strength mixed-mode ICs. The paper proposes a fast semi-analytical technique for substrate analysis, which is claimed to be accelerated for use within optimization loops. The algorithm at the heart of the optimization technique uses the results from [1], which is also explained in detail in this paper. The algorithm explained generates a network accurately modeling contact-to-contact resistance in arbitrarily-shaped doping regions. Techniques to improve speed of operation by trading off on circuit complexity is discussed. The authors discuss

in detail the sensitivities of all the network components with respect to a number of technology parameters using the Green's function expressions as before. The sensitivity analysis as mentioned has quite a few advantages. It allows the evaluation of the impact of slight imperfections in the fabrication process on the circuit's performance and, ultimately, its yield. It also can be used as a quality factor for the selection of the best cost-effective technology on the basis of a class of circuits one want to fabricate with given specifications. Further, the analysis can be used during optimization to help the decision process providing guidance to the best possible improvement. The authors conclude that the effects of technology migration/scaling can be carried out efficiently for a given chip without the need of performing a large number of complete substrate extractions. The paper gives a detailed account of the algorithm underlying the sensitivity analysis based optimization technique. Also a number of design optimization problems are presented and the suitability of the approach is explained for a specific mixed-mode IC designed with substrate-aware optimization technique in CMOS process.

Though there are many publications available today on different aspects of substrate coupling, my focus is mainly on understanding the research in modeling of substrate noise and circuit analysis based on the models. An efficient modeling approach on substrate noise analysis is discussed in [9] for specifically heavily doped CMOS process. The model is based on Z parameters that are scalable with contact separation and size. The paper also presents validation results with simulation and experimental data. For the specific case of highly doped substrate, the authors have come up with a prediction scheme to determine the effective Z_{11} and and Z_{12} values between contacts of any dimension based on the area, perimeter and spacing between the contacts along with some empirical and process dependent fitting parameters. This technique effectively helps in computing the equivalent resistances between contacts for any shape and size. The authors show that, in the Z domain , the resulting Z parameters help in generating a dense Z-matrix of size $N \times N$ where N is the number of contacts, thereby maintaining the one-to-one relationship between every contact with one another without losing any vital inter-relation between any two contacts. The Z-domain macromodel formulation also aides in improved com-

putational efficiency and accuracy. The effective resistance is eventually determined from the Z parameters computed using the formulas developed for the model. For square contacts, the $1/Z_{11}$ increases quadratically with the contact width and Z_{12} is an exponential function of the contact spacing. The resulting relationship in the Z domain translated to mathematical formulas for computing the Z domain results based on the parameters as mentioned earlier. The resulting equations for $Z_1 1$ and Z_{12} are are given by equations 2.1 and 2.2.

$$Z_{11} = \frac{1}{K_1 Area + K_2 Perimeter + K_3} \tag{2.1}$$

$$Z_{12} = \alpha e^{-\beta Z} \tag{2.2}$$

where, K_1, K_2 and K_3 are empirical fitting parameters and β is a process dependent parameter and α is the value of Z_{12} when the spacing between the contacts is zero. Application examples showing the advantages of Z-domain macromodeling have been discussed. The author compares the results of non-scalable techniques and scalable techniques that they have developed in proving the accuracy and computational efficiency of the scalable technique.

2.3 Summary

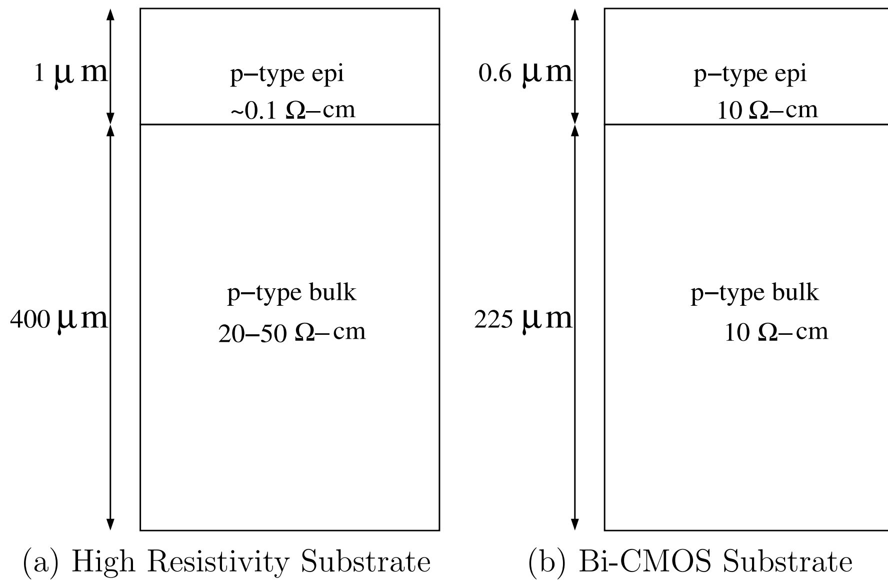
As mentioned earlier, many more papers addressing various issues of substrate noise coupling have been available in many journals. What was provided here is a survey of some journals related to the work that undertaken in this thesis. Hence the survey is not exhaustive with regards to the field of integrated circuit design under consideration.

Chapter 3

Mechanism of Noise Coupling in Substrate

Substrate types of interest in RF integrated circuit manufacturing these days are the high-resistivity substrates used in BJT-based IC designs, the substrate type for Bi-CMOS based IC designs and Deep N-well Low-Resistivity substrates for CMOS based IC. The substrate considered in the current research are the High-Resistivity substrate and the typical substrate used in Bi-CMOS based designs. The cross-section of the substrates for these two cases are shown in Figure 3.1(a) and Figure 3.1(b) respectively. As can be seen, the high-resistivity substrates are composed of a lightly-doped bulk region which is about $200 - 400\mu$m thick and a thin epi-layer which has a low resistivity. As can be seen in Figure 3.1(b), the resistivity of the bulk region for Bi-CMOS circuit substrates are half-way between typical High-Resistivity and Low-Resistivity substrates. This is consistent with the need to have both CMOS and BJT based circuits on a single substrate. The bulk region is medium-doped which is about $100 - 400\mu$m thick and the epi-layer is typically less than a μm thick. CMOS based circuits have parasitic latch-up issues which are well controlled using Low-Resistivity substrates while High-Resistivity substrates are better suited for BJT based circuits. Modeling the complex substrate layers of the Deep N-well topology was not possible and hence was not considered in this research.

The Mechanism for substrate noise injection and reception in different devices and



(a) High Resistivity Substrate (b) Bi-CMOS Substrate

Figure 3.1: Cross Section of Substrates.

the transmission mechanisms in substrates are discussed in this chapter.

3.1 Sources of Noise Injection

Different types of Active and Passive devices are used in Silicon Integrated circuits. Typical active devices include Bipolar Junction Transistor (BJT), MOS transistors and Diodes. Typical passive components include resistors, capacitors, inductors and interconnects. Local wells and diffusion structures are also passive structures.

3.1.1 Injection Mechanism in Active Devices

Bipolar Junction Devices and Diodes

A cross section of a bipolar npn transistor is shown in Figure 3.2. These devices interact with the substrate through the collector-to-bulk junction capacitance (C_{CS}). The value depends on the substrate and collector doping levels, as well as the bias

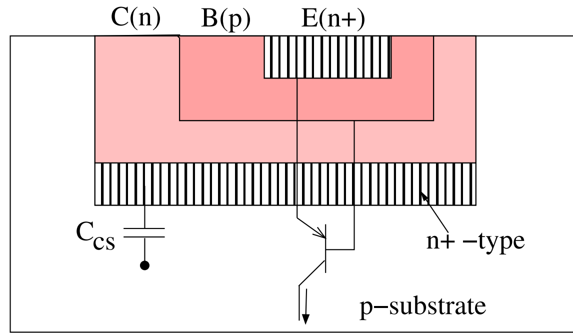


Figure 3.2: Cross section of an NPN transistor with parasitics.

level of the collector with respect to the substrate:

$$C_{cs} = \sqrt{\frac{q\varepsilon}{2\left(\Psi_{bi} + V_{cs}\right)} \frac{N_C N_S}{N_C + N_S}} \tag{3.1}$$

where N_C and N_S are the collector and the substrate doping densities respectively, Ψ_{bi} is the built-in potential of the pn junction, and V_{cs} is the collector-to-substrate bias voltage. Another mechanism for noise injection into the substrate from a BJT is when the device approaches the saturation region of operation. When the base begins to be forward biased with respect to the collector, the parasitic pnp transistor shown in Figure 3.2 begins to enter its forward active region of operation. The base of the npn device acts as the emitter of the pnp, the collector as its base and the p-substrate as its collector. The parasitic pnp device is in the cutoff region when the npn transistor is in the forward-active mode. The forward gain of this device is small, since the parasitic base (the npn collector) thickness is quite large.

Lateral pnp transistors inject noise into the substrate through the base-to-substrate capacitance. This is evident as shown in Figure 3.3. In vertical pnp devices the substrate is the collector node, see Figure 3.4. Hence these devices can act as significant substrate noise injectors, and this may degrade the performance of the circuit due to high resistive nature of the substrate. To avoid this, a sufficiently low impedance path must be provided near the device in order to collect the current through the substrate [8].

Diodes are typically fabricated by tying together the base and the collector of bipo-

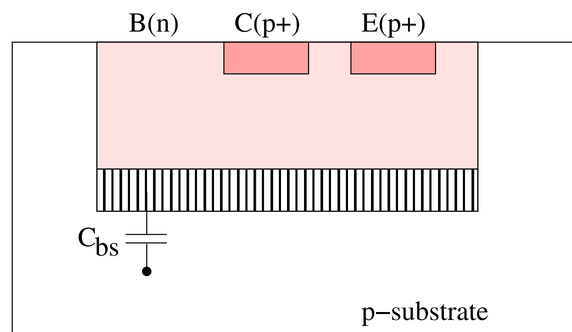


Figure 3.3: Cross section of a lateral PNP transistor with parasitics.

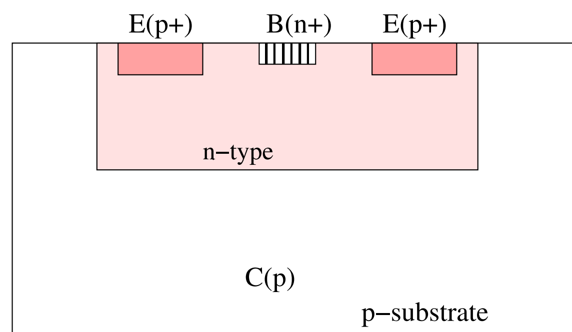


Figure 3.4: Cross section of a vertical PNP transistor with parasitics.

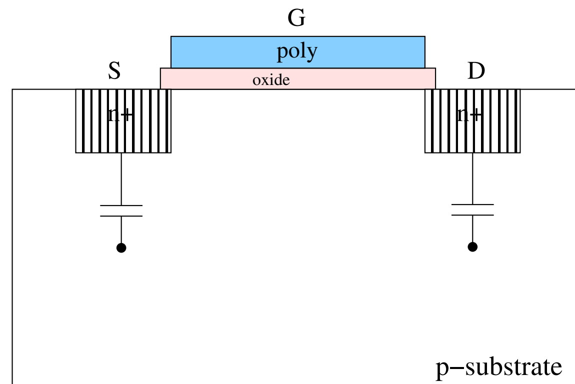


Figure 3.5: Cross section of a NMOS transistor with parasitics.

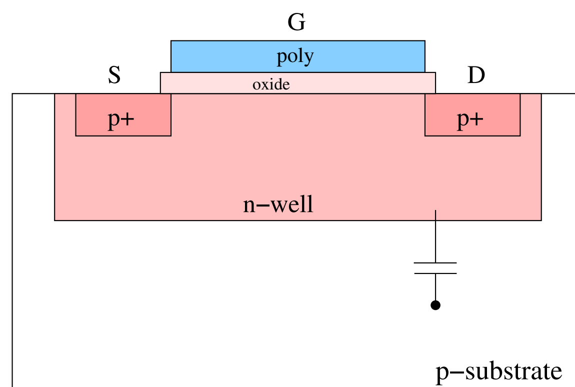


Figure 3.6: Cross section of a PMOS transistor with parasitics.

lar npn transistors. Substrate current injection in these devices takes place through the collector-to-substrate junction capacitance as discussed before.

MOS Devices

A cross section of the MOS devices are shown in Figures 3.5 and 3.6. The figures depict an n-well process. In such a process, NMOS devices interact directly with the substrate through the source/drain-to-substrate capacitance, modeled as CJ0 and CJSW. Additionally, hot-electron effects also cause injection of majority-carriers into substrate. Hot-electron effects result when the field in the depleted drain-end of the transistor becomes large enough to cause impact ionization and generate electron-

hole pairs. Its been found that hot-electron based induced substrate currents are the dominant cause of substrate noise in NMOSFETs up to at least a hundred megahertz. Short channel lengths of current device technologies can still worsen the problem of substrate noise injection due to hot-electron effect.

The nature of current injection due to capacitive coupling and avalanche induced currents is different because hot-electron induced currents are always injected into the substrate. In a switching CMOS inverter, hot-electron induced current will always be injected into the substrate while the capacitance induced current will alternate based on the transition from $1-0$ and $0-1$. Hence hot-electron induced currents will possess large even order harmonics of the fundamental and DC components. The presence of DC components in any substrate current can potentially be very harmful to circuit operation. This will cause threshold variation in the devices and also lead to increase in minority-carrier injection due to partial forward biasing of the device-to-substrate junctions. Hot electron related effects must hence be given serious consideration in circuits where signal levels are expected to be high.

For small-signal analysis, the effect of the hot-electron induced current can be modeled as a drain-to-body transconductance g_{db}, [8], given by

$$g_{db} = \frac{\partial I_{dub}}{\partial V_D} = \frac{K_2 I_{sub}}{\left(V_{ds} - V_{dsat}\right)^2}. \tag{3.2}$$

The major effects of this parameter on small-signal circuit analysis is that this term appears in parallel with the r_o of the device and tends to lower the output impedance of the transistor.

Hot-electron induced substrate currents in PMOS devices are considerably smaller than in comparably sized NMOS devices due to a lower hole ionization-coefficient. Further PMOS devices generally have locally grounded wells. However proper grounding of the well is necessary or else there will be a variation in the well potential with respect to the substrate potential. The well with a large reverse-biased well-to-substrate capacitance can act as a large injector and can cause significant substrate noise injection.

In addition, as discussed earlier, the reverse-biased pn junctions formed by these

devices with the substrates also exhibit a steady DC leakage current. This current consists of carriers which are swept across the depletion barrier in the directions of the electric field. Electrons are injected into the n-region and holes into the p-region under the action of the field. Hence the substrate current induced by this mechanism is a majority-carrier drift current.

3.1.2 Injection Mechanism in Passive On-Chip Components

The on-chip passive components in typical processes are shown in Figure 3.7. These include resistors, capacitors, inductors and local diffusions.

Resistors in current processes are either poly-type or diffused. Poly resistors have a comparatively smaller parasitic capacitance to the substrate than diffusion resistors. Thus diffusion resistors inject more noise into the substrate than poly resistors for the same dimensions. If one end of the resistor is connected to an AC ground then the current injected into the substrate at low-frequencies, due to a voltage V_{in} applied at the other end is given by

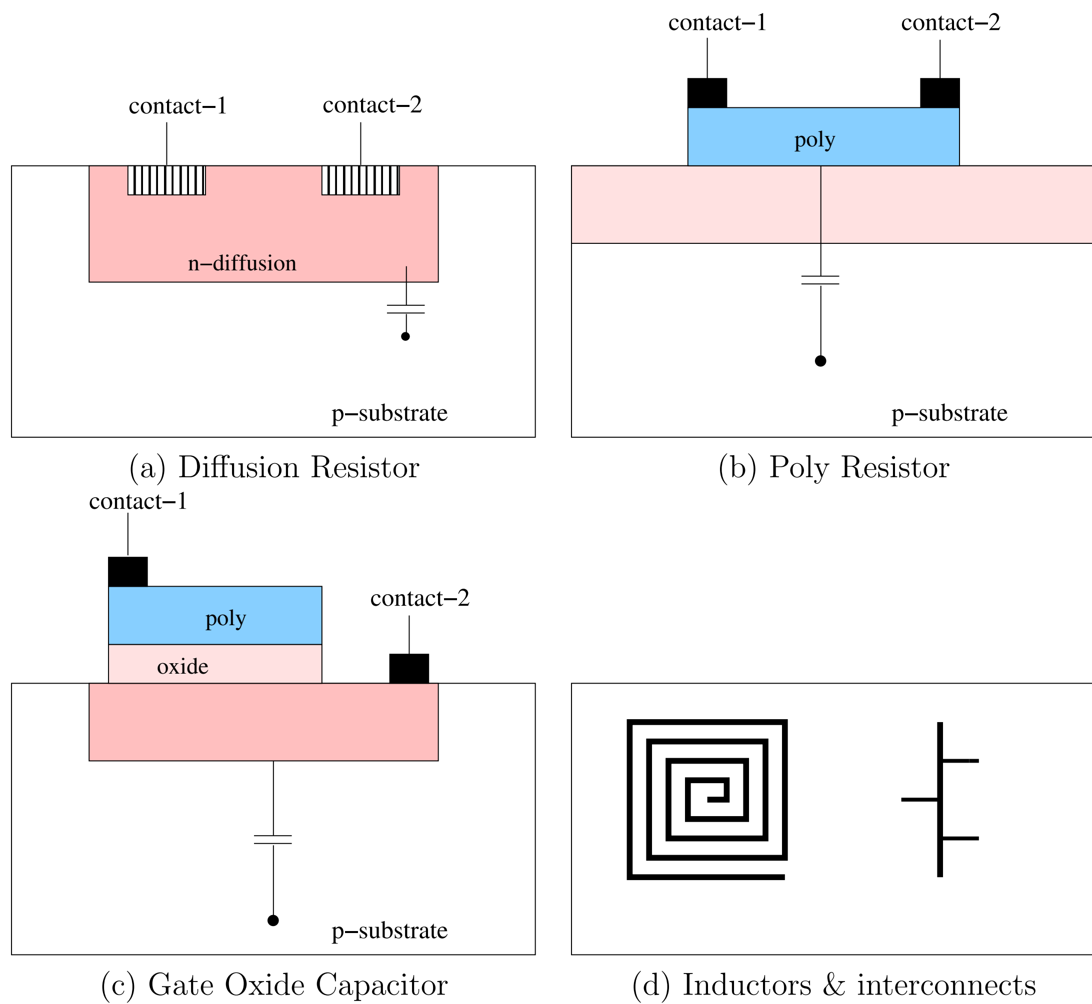
$$I = \sqrt{\frac{j\omega C}{R}} \tanh\left(\frac{\sqrt{j\omega RCL}}{2}\right) V_{in} \tag{3.3}$$

where C is the per unit length capacitance of the resistor, R is the per unit length resistance and L is the length of the resistor. At high frequencies, the injected substrate current has a $f^{0.5}$ dependence. This formula is obtained by modeling the resistor as a dissipative transmission line provided in literatures.

Capacitors can be either poly-to-poly, metal-to-poly or poly-to-substrate types. Metal-to-metal capacitors have the largest ratio of the parasitic capacitance to the substrate for a given capacitance. Hence if these devices are used for implementing large on-chip capacitors, they can act as significant substrate noise-injectors.

On-chip inductors and interconnects inject noise into the substrate through the parasitic oxide capacitance with the substrate. The substrate parasitic can lead to lowering of the inductor quality factor. Thus the substrate parasitics must be modeled to obtain an accurate prediction of inductor performance.

Local diffusions in the substrate can be p or n-type. N-type diffusions inject noise



(a) Diffusion Resistor

(b) Poly Resistor

(c) Gate Oxide Capacitor

(d) Inductors & interconnects

Figure 3.7: Cross section of various on-chip parasitic components.

through a reverse bias capacitance. P-type diffusions are often used as substrate taps or guard rings. They serve to tie down the substrate to a desired potential. If designed improperly these diffusions can inject very high levels of noise into the substrate, as they act as wide ground-planes on the substrate and any voltage bounce on these diffusions is conveyed throughout their extent on the chip through a very low impedance path. Guard rings will be further discussed in the following chapter.

3.2 Reception of Substrate Noise

The reception of noise by most devices on the surface takes place through capacitive sensing.

The junction with the substrate in lateral pnp devices is formed by the n-type region. If the pnp device is used in a gain stage, then the base of the device must be carefully shielded, or connected to a low impedance node. Otherwise the coupled substrate noise on the base will be amplified by the gain of the circuit.

In addition to capacitive pickup through the source and drain depletion junctions, MOS devices also exhibit substrate interaction through body effect. As we know, the threshold voltage of a MOS transistor is a strong function of the substrate potential. The substrate voltage dependence on V_T for a given impurity concentration N_A is given by [8]

$$V_T = V_{T0} + \frac{\sqrt{2q\varepsilon N_A}}{C_{ox}}\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right) \tag{3.4}$$

where V_T is the threshold voltage, ε is the permittivity of silicon, C_{ox} is the per unit area oxide capacitance, $2\phi_f$ is the surface inversion potential, and V_{SB} is the source-to-body potential. The body effect makes the drain current dependent on the substrate potential through the threshold voltage. This drain current due to substrate potential can be represented as a bulk-to-drain transconductance, g_{mb} in a small signal model. In typical processes as shown in [8], the ratio of g_{mb} to g_m varies from 0.1 to 0.3, where g_m is the transconductance of a MOS transistor. Thus, the parasitic body-to-drain gain is lower than gate-to-drain gain by a factor of say $11 - 20$ dB only.

Hence, the body effect in MOSFETs makes the devices especially vulnerable to substrate noise reception at lower and higher frequencies. While the capacitive pickup, exhibited by most of the devices, become significant only at relatively high frequencies, the body effect can be a issue to consider at low frequencies.

3.3 Substrate Noise Transmission

Substrates act as the media for coupling of noise from one device to another. Thus, to understand the phenomenon of substrate coupling, it is essential to determine the dominant mechanisms for current flow in the substrate. This section describes the different mechanisms through which substrate noise is coupled and their dependence on various substrate materials interpreted as circuit elements.

3.3.1 Analysis of Simple Substrate Models

If substrates are modeled as a lossy dielectric, then the distributed form of the Ohm's law can be made applicable to these substrates. It is given by,

$$\mathrm{J} = (\sigma + \mathrm{j}\omega\varepsilon)\mathrm{E} \tag{3.5}$$

where J is the current density in the substrate (A/cm^2), E is the electric field (V/cm), σ is the conductivity and ε is the dielectric permittivity of silicon. The term within the brace in Equation 3.5 represents the distributed impedance relating the electric field to the current density. For frequencies up to a few GHz, the impedance is purely resistive based on the conductive nature of the substrate. For typical substrates, the conductive nature is such that the substrate acts as a purely resistive networks for frequencies up to 5 GHz. However for frequencies above 5 GHz, the analysis is not based on the simpler electrostatic approach but by solving Maxwell's equations discussed later in this chapter. The above equation considers current flow only due to drift currents which are field induced due to majority carrier conduction.

The flow of minority carriers is due to diffusion currents which are more complex

to model. However, minority-carriers, once injected into the substrate, can exist for long periods of time (carrier lifetime) and cause significant local variations in conductivity. And, a large injection of minority-carriers into the substrate usually indicates a fault condition, as this occurs when a device-to-substrate junction is turned on. Hence, any minority-carrier injection through the substrate is more a fault on the design of the circuit than a substrate noise issue and hence, has not been considered for further analysis.

3.3.2 High-Frequency Characterization of Substrates

At high Frequencies above 5 GHz, the electrostatic assumption of modeling the substrate is not totally right. Depending on the frequency of the signal, three different modes can be observed in the substrate [11]. These modes are the quasi-TEM modes, the slow-wave modes and the skin-effect modes. The quasi-TEM modes occur when the susceptibility of the silicon layer is much higher than its conductivity. The SiO_2-Si behave life a multilayered dielectric. The skin-effect modes also appear at high frequencies when the vertical dimensions of the Si layers become comparable to the skin depth. At frequencies where these modes are not dominant, the substrate can be modeled as a distributed resistance.

The interesting feature is that the model closely follows the electrostatic approach discussed earlier. The models for the slow-wave mode and the quasi-TEM mode includes the substrate effects as a distributed resistance. In the skin-effect mode the substrate acts as a think lossy ground-plane. The skin-effect mode is dominant for substrates with resistivities less than 0.01 Ω-cm. Substrates with resistivities greater than this value exhibit the other two modes, with the quasi-TEM being the dominant one at higher frequencies.

Chapter 4

Substrate Coupling in Integrated Circuits

In this chapter, we develop layout topology that represent common circuit types to understand how they respond to coupling provided by different substrate models. To do this, a detailed analysis has to be done on the substrate model to characterize the model for circuit level analysis. Analysis of various parameters involved in substrate noise coupling at the substrate level and the components in circuits is studied. Techniques to minimize the effects of coupling given a certain substrate type has been developed.

As mentioned in the previous chapter, contacts on a substrate can be modeled as a pure resistance network for frequencies up to 10 GHz. Since this resistance model is necessary for circuit level analysis of the coupling in different layout topologies, the need for substrate extraction is necessary for utilizing the model in simulators. Hence, the basic task is to correctly extract the resistance network for different substrate types under consideration.

The tool used for this purpose is Agilent's ADS Momentum. Momentum is one of the tools in ADS that can be used to build various RF components, passive and active on substrates to analyze and understand the functionality of the same. Hence, the process of substrate extraction for various layout topologies were carried out using this tool. A detailed information on the tool and its application can be found in [14].

The correctness of the results provided by the tool for this particular purpose was determined by comparison of extracted results from Momentum for simple single contact topologies with the published results in papers [1, 2, 4] based on Numerical Analysis. The closeness in results prompted the choice of using the tool for further analysis.

The accuracy of the extracted results are based on the correctness with which the exact substrate model is built. However, there are certain topologies like the Deep N-well which are difficult to be built taking into consideration all parasitic effects. Hence analysis of substrates have been done to the scope to which the simulator responds correctly.

Two commonly used substrate types in current RF Integrated Circuits and its effects on substrate coupling are considered in this research. The complexity of the model is within the scope of the tool used. They are the High Resistivity substrate and substrate used in Bi-CMOS designs. As mentioned earlier, RF CMOS circuits use Deep N-well substrates for better circuit functioning, whose substrate topology was beyond the scope of the tool used, for this work.

The substrate model used in the analysis is as shown in Figure 4.1. The depth of the bulk and epi-layer and the resistivity information for each of the layer is as mentioned in the diagram.

Before getting into the details with different layout topologies, simple contacts representing substrate connection to active layers were built on the substrate model. This was done to simulate and extract the resistive network created by the contact with the substrate. Simulation was done to extract the contact to back plane resistance and resistance between adjacent contacts. For this purpose, single contact and double contact layout were built respectively. The extracted results were used to understand the distribution of resistance in the two different substrates and hence analyze their distribution on different layout schemes.

Further, additional layout techniques like adding guard ring was considered to understand their benefits on coupling in the two substrates.

Also, as a second purpose, the extracted resistive network was used in ADice, a circuit simulator similar to Spice and fREEDA, to determine the substrate coupling

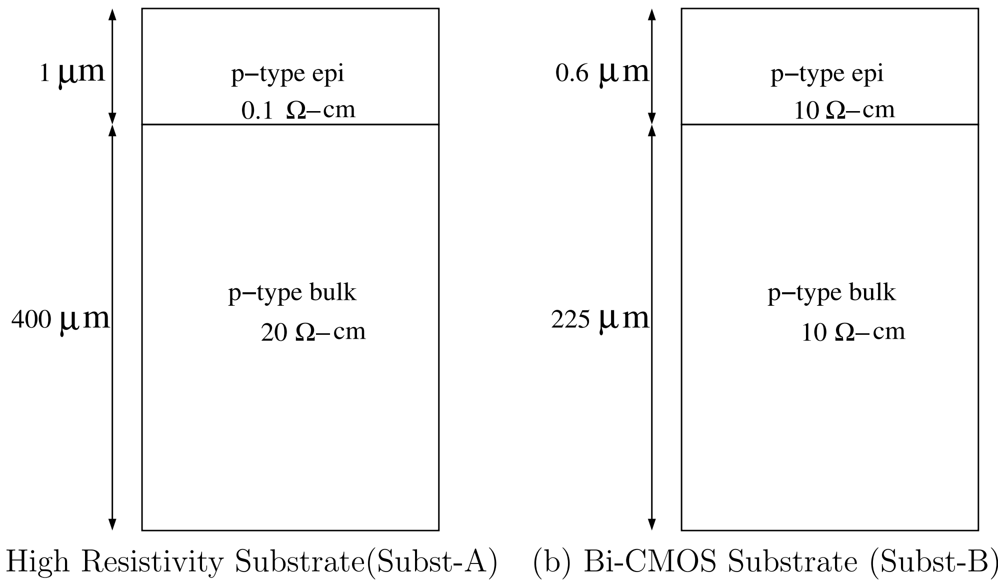
between contacts computed in terms of gain between between voltage coupled and voltage received. Various circuit parameters in the simulator were tweaked to understand the variations in substrate coupling. The different schematic used in the simulator will be presented and discussed in detail. Circuit level techniques to improve isolation will be discussed as part of this analysis.

This chapter is subdivided into the following sections. The first section deals with the general topology of the substrates under consideration and its benefit on the circuit built on it. The substrate resistance behavior of the substrates based on the single contact and double contact model is analyzed in the following two sections. This is followed by studying the effect of Guard Ring on the substrate resistance model. Following this the circuit level analysis of computing isolation in single ended topologies is discussed. Substrate coupling is strongly dependent on the circuit components on chip, grounding schemes etc. Each of this is presented individually with simulation results. The penultimate section deals with analysis of substrate coupling in differential topology using analytical models developed. The effects of layout spacing, component mismatches, guard ring addition on isolation are analyzed and presented for design choices. A summary of results from the thesis is provided finally.

4.1 Substrate Models

Let us begin the analysis with understanding the cross section of the substrates under analysis followed by determining the distribution of resistance in each of the substrates using a single contact and double contact models. The result of this analysis help us in getting a broader picture of the substrates in developing analytical model for understanding its effect on different circuit topologies to be considered.

Figure 4.1 represents the layer information of the two substrates to be used for analysis. It is the same as the representation in the earlier chapter, but the substrate information is more specific with respect to physical dimension information used for simulation purposes. The high resistivity substrate (Figure 4.1(a)) consists of a thin epi-layer of thickness 1μm and resistivity 0.1 Ω-cm and a bulk of thickness 400μm with a resistivity of 20 Ω-cm. This can serve as a substrate for BiCMOS too as the



(a) High Resistivity Substrate(Subst-A) (b) Bi-CMOS Substrate (Subst-B)

Figure 4.1: Cross Section of Substrates.

low resistivity epi can serve as a channel stop. The second substrate is a substrate whose bulk resistivity, as discussed in the previous chapter, is half way between a high resistivity and a typical low-resistivity substrate, for building BiCMOS circuits. The resistivity of the substrate is defined by the resistivity in the bulk region of the substrate. The second substrate considered here, has a epi-layer of thickness 0.6μm and a bulk of thickness 225μm each having the same resistivity of 10 Ω-cm. In typical CMOS based circuits, the substrates have a very low resistive bulk, a high resistivity epi and a thin channel stop low resistive implant on top [1, 12]. However, to build good BJT devices with reasonably good device characteristics, the base of the BJT should be doped to the optimum level for which there must be a finite amount of doping in the substrate. Hence to build a BiCMOS device, there must be a trade-off in the doping levels of the substrate to build CMOS and BJT.

In the forthcoming discussions in the chapter, the High Resistivity substrate will be referred by the name Subst-A and the BiCMOS based substrate will be referred by the name Subst-B for easy understanding.

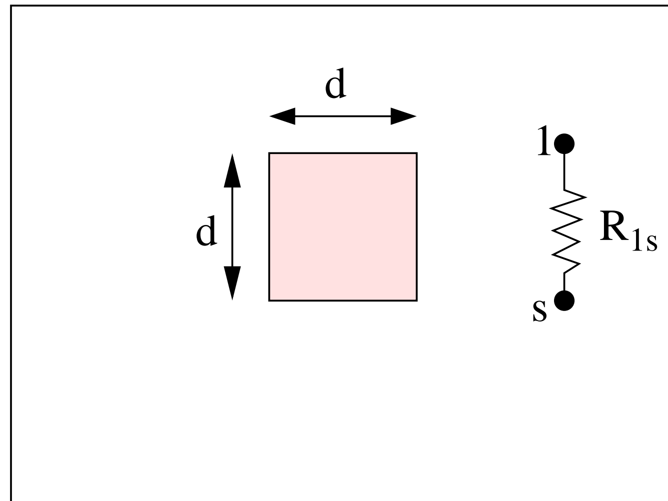


Figure 4.2: Single Contact layout on a square substrate

4.2 Substrate Resistance Modeling

This analysis deals with understanding the behavior of the substrate resistance as function of contact area and distance between contacts. The model of the substrates provided earlier was built on Momentum and simulation was done to extract the substrate resistance information and pattern.

4.2.1 Single Contact Substrate Model Substrate

The resistance of a single square surface-contact, see Figure 4.2, to the substrate back plane for Subst-A and Subst-B is shown in Figure 4.3. The contact is placed at the center of the substrate. The resistance to the back plane shows a weak logarithmic dependence on the dimension of the contact for the contact on Subst-A, while the resistance has a reasonably good dependence on the contact dimension ($\ln(R) \propto -\ln(d)$) for the contact on Subst-B. The reason for this difference can be explained as follows. In the case of a high-resistivity substrate, the low-resistivity epi-layer on the surface of the thick high-resistivity bulk region tends to increase the fringing fields. Thus the effective contact area appears to be much greater than the physical contact area. This explains the weak dependence of the resistance to the con-

tact sizing in Subst-A. In Subst-B the epi-layer is equally resistive (low doped than the epi in High resistivity) as the bulk. Here there is no significant fringing fields compared to the high resistivity type. Hence the resistance to the back plane is more dependent on the size of the contact as can be seen by the good inverse dependence of the back plane resistance to the contact dimension.

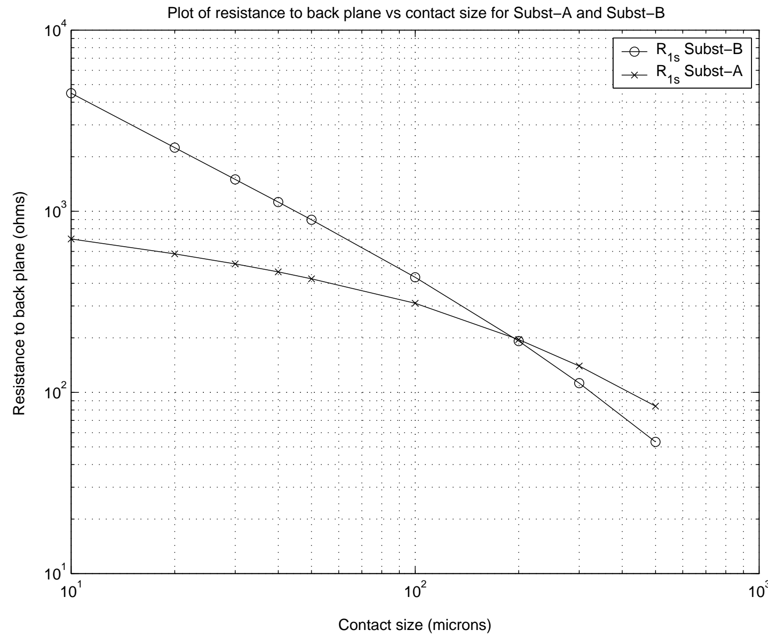


Figure 4.3: Plot of back-gate resistance to contact size of a single contact in Subst-A and Subst-B

4.2.2 Two Contact Substrate Model

Now considering a two-contact problem, there is an additional third resistance element in addition to the two back plane resistance from the two contacts. That is the resistance between the contacts. The layout for the problem is as shown in Figure 4.4 and the equivalent schematic model representing the three resistances, R_{1subst} and R_{1subst} between the contact and the back plane and R_{12} between the contacts is shown in Figure 4.5. This problem was considered to understand how the resistance between two contacts vary with increasing separation between contacts. An arbitrary contact of 20 μm per side square contact has been chosen.

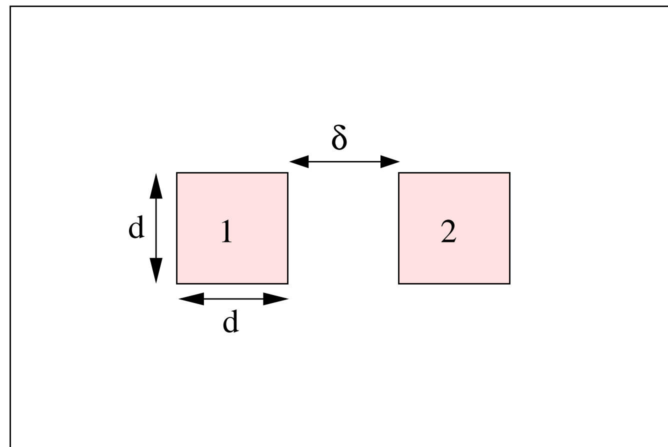


Figure 4.4: Two contact layout for substrate resistance analysis.

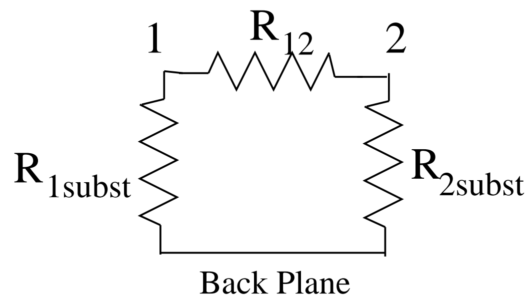


Figure 4.5: Schematic representation of the two contact single ended layout.

The plots of the element resistance as a function of separation between contacts for Subst-A is shown in Figure 4.6 while Figure 4.7 shows the same for Subst-B. Distance δ between the contacts is the X-separation between the contacts. The contacts are assumed to be equidistant from the center of the substrate for any δ. Since the resistance from each of the contact to the back plane is the same, only one contact to back plane resistance is plotted. The resistance between the contacts in Subst-A, increases monotonically as can be expected. The curve shows a quadratic dependence on the distance between contacts. The constant in the equation will represent the contact to back plane resistance of a contact with twice the area which is the case when the contacts are connected together when the separation between them becomes zero. The resistance to the back-plane decreases with increase in X-separation. It is

large when the two contacts are close, which implies that a significant portion of the current flow is through the surface region. Comparing the back plane resistance plots for a single contact and dual contact structure, we see no major factor controlling the resistance to the back plane in a two contact problem. Even for large separation between contacts, there is some finite amount of current flow in the surface and some shared by the bulk. Otherwise, we would expect a flattened resistance plot to the back plane at a distance where the current flow is completely through the bulk. Hence using techniques to retard surface current flow would aid better isolation in this substrate.

In Subst-B, the resistance between contacts is much greater compared to the equivalent in Subst-A by a magnitude of 10 as the distance between the contacts increases. As seen in the plot, the variation is exponential as the plot on the semi-log graph is linear for a major part of the curve. The resistance to the back-plane in 4.7(b) decreases similar to that of in Subst-A, but the effective resistance starts to flatten after a certain critical distance as at this point, majority of the current flow is through the bulk. This will directly affect the isolation if the back plane ground connections are not proper. From the plot,

$$R_{12}(x) = \alpha e^{\beta x} \tag{4.1}$$

where α and β are fitting parameters of the curve showing the resistance between contact in Subst-B. α will be a function of the contact area and the perimeter of the contact. This effective resistance will be the resistance of a contact to back plane that is twice the area. Now, β will be the effective process dependent parameter since the rate at which the resistance increases depends on the resistivity of the substrate and the sizing. Hence the fitting parameters α and β need to be determined from experimental simulation for the specific contact size used. No two resistance between contact for two different contact area will be similar because the fitting parameter α is a function of contact area [12].

As the separation tends to infinity, the effective back plane resistance will become the resistance of the single contact. This is shown by the flatness in the resistance curve in the plot of Figure 4.7(b). For very small separation between contacts, the ef-

fective resistance to back plane for one contact will also be dependent on the resistance between the contacts. Hence in a two contact problem, based on the Y parameter of the 2-port network and the contact to back plane resistance of the single contact structure, we can deduce that

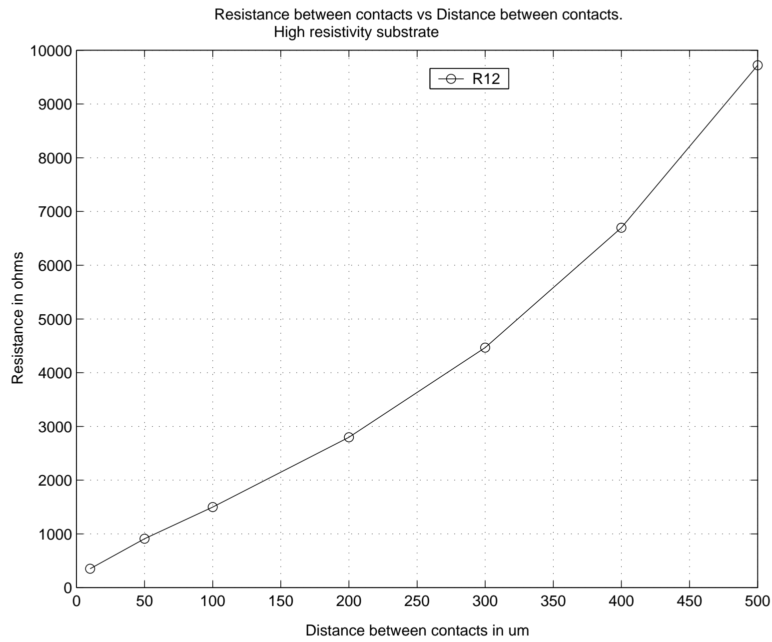
$$R_{1subst}(x) = \frac{R_{11}}{2} - \frac{1}{R_{12}(x)} + \frac{R_{11}}{2}\sqrt{1 + 4\left(\frac{1}{R_{11}}\right)^2\left(\frac{1}{R_{12}(x)}\right)^2} \quad (4.2)$$

where, R_{11} is the resistance to the back plane for a contact in a single contact structure. The size of the contact being the same as that of a contact used in the two contact structure. This can be determined from the plot between resistance and contact sizing shown in Figure 4.3 for Subst-B. R_{12}(x) is the effective resistance between contact for a certain separation X which can be determined using Equation 4.1. From this equation we can see that, as the distance between contacts tend towards infinity, the effective resistance of the contact to back plane will be R_{11}. Figure 4.7 shows the plot of resistance between contact and resistance to back plane for Subst-B. The curve from simulated result and the curve from the model above are shown and they match very well to the result.

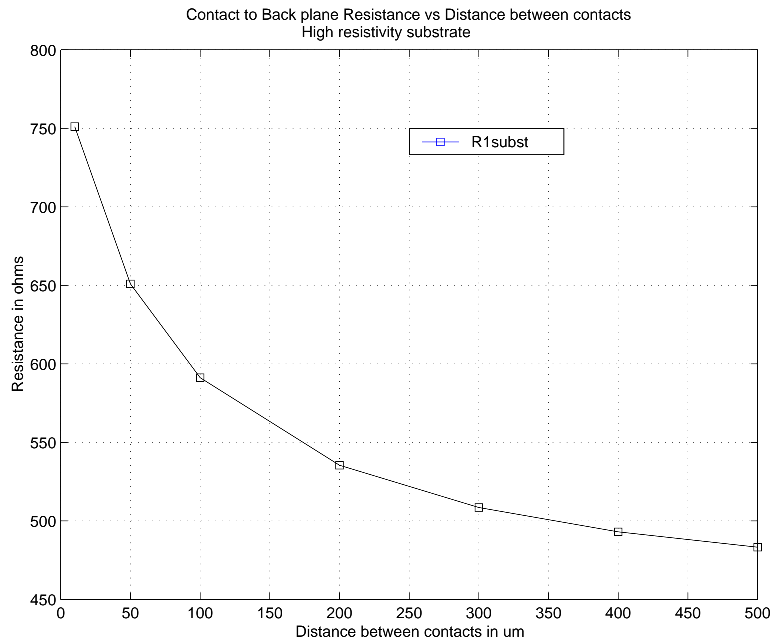
4.2.3 Guard Ring Effect on Two Contact Model of Substrate

Guard Rings surrounding devices are normally formed of P-diffusion elements on P-type substrates. The guard rings are connected to ground through bond-wires which have a finite amount of inductance. The benefit of the guard ring is that, it creates a shorter path for the substrate current to ground thereby improving isolation between two contacts that are independent of each other.

The effect of an additional Guard Ring around a single contact on the resistance network is analyzed here. The layout for the same is shown in Figure 4.8. A plot of contact to back-plane resistance and contact to contact resistance for the two substrate type, Subst-A and Subst-B is shown in Figures 4.9 and 4.10 respectively. In the case of Subst-A, as we can see, the resistance between the injector contact(1) and receiver contact(2), see Figure 4.9(a), has increased almost 10 times with the addition of a Guard Ring compared to the case without Guard Ring. The increase is

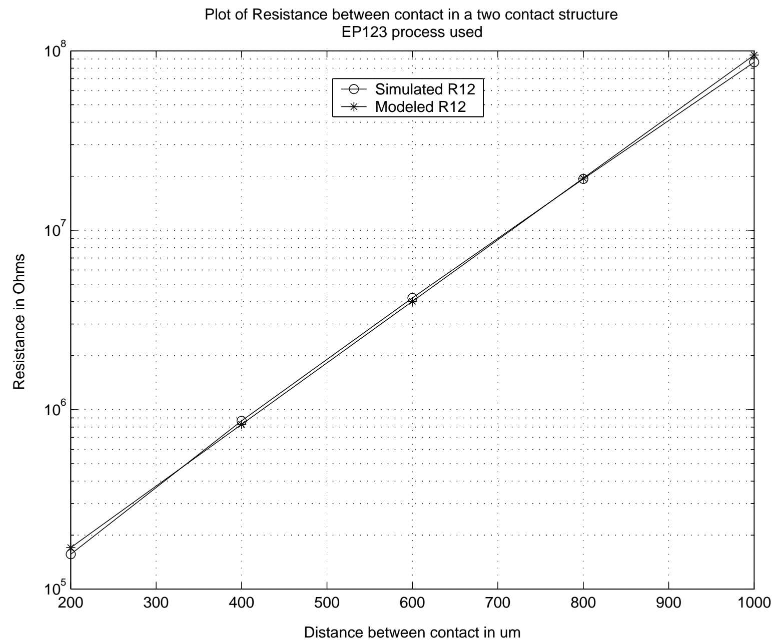


(a)

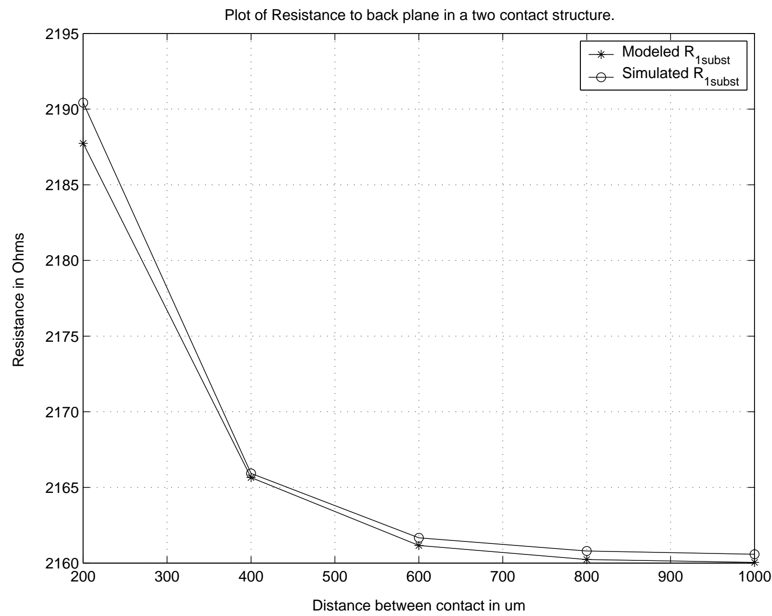


(b)

Figure 4.6: Plot of resistance (a) between contacts and (b) contact and back plane, in a two contact analysis in Subst-A



(a)



(b)

Figure 4.7: Plot of resistance (a)between contacts and (b) between contact and back plane, in a two contact analysis in Subst-B

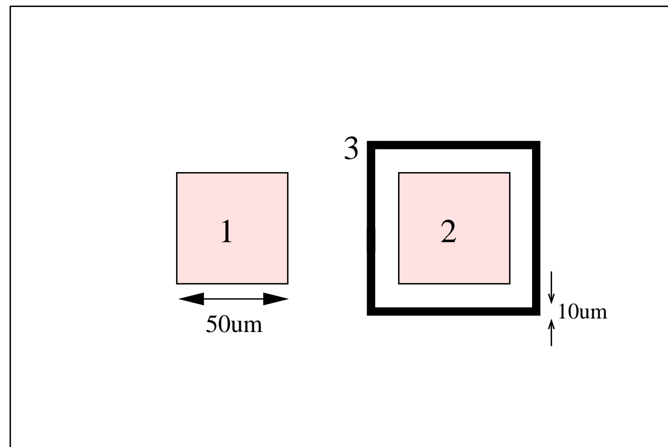
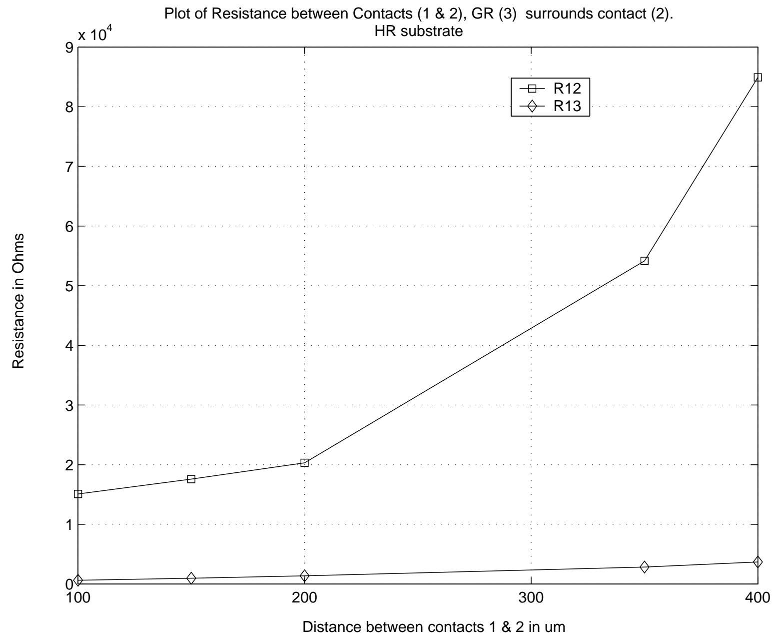
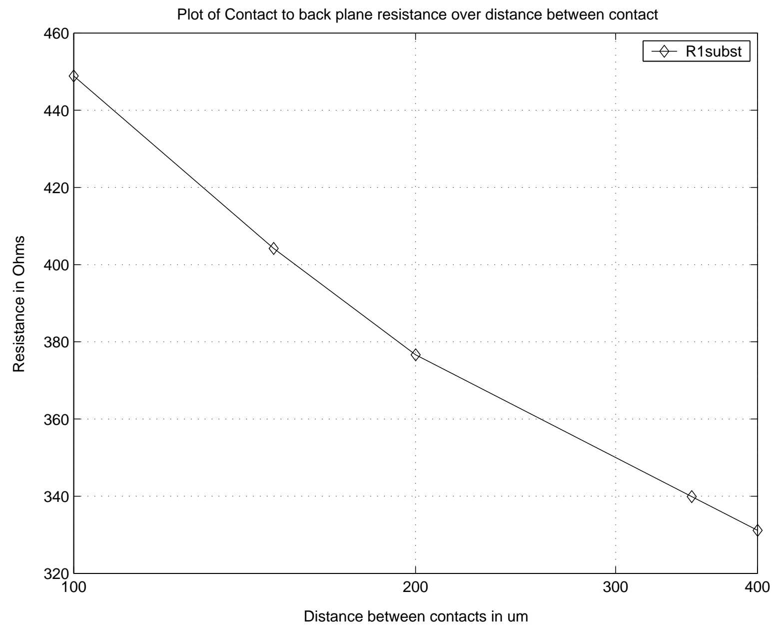


Figure 4.8: Two contact layout with guard ring surrounding the receiver.

as expected monotonic and the resistance grows faster with distance as the relation is almost cubic. This is in expected lines since significant current flow is on the surface through the low resistivity epi. The surface area of the guard ring is large enough to have a smaller resistance path to ground. This problem is further alleviated by the guard ring inductance to ground in packages. The Guard Ring acts as a current sink around the receiver contact and with a high resistivity bulk, the contact to back plane resistance is large for the contact surrounded by the Guard Ring and is no more a concern. The Guard Ring does the job of isolating the contact it surrounds to a significant extent. The contact to back-plane resistance in Figure 4.9(b), however, is still a monotonically decreasing function. With Guard Ring, the effective isolation is determined by the decrease in resistance between the injector contact and the Guard Ring. Since the Guard Ring is closer to the injector contact and has a lesser resistance path to ground for the surface currents, it acts as a better receiver. Hence, the better the grounding of the Guard Ring, the lesser is the resistance between injector and Guard Ring and larger the isolation between the contacts. From the values of the resistance between contacts(1) and (2), we can come to the conclusion that with an addition of a Guard Ring, for reasonably good grounding schemes, an increased isolation of at least 15 dB can be achieved just at the substrate level. This can be further increased with better grounding schemes for the Guard Rings in the

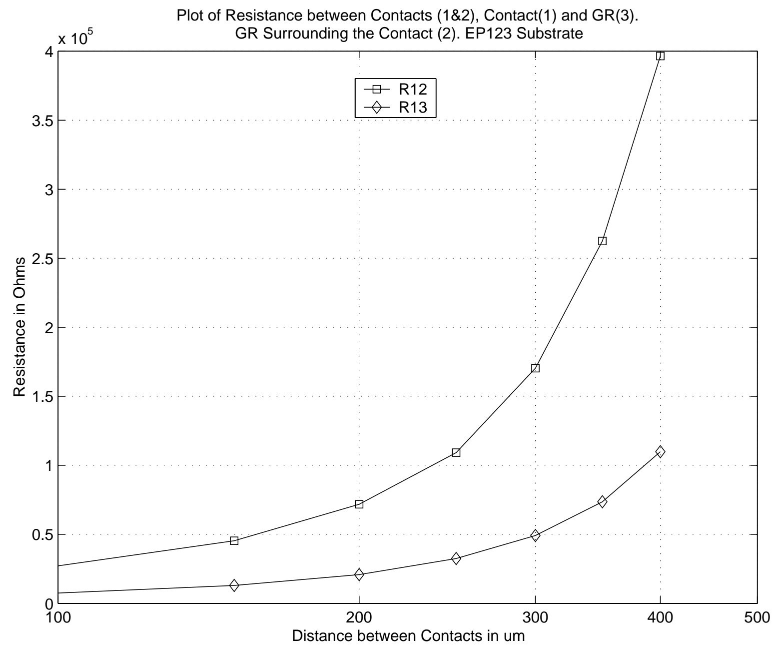


(a)

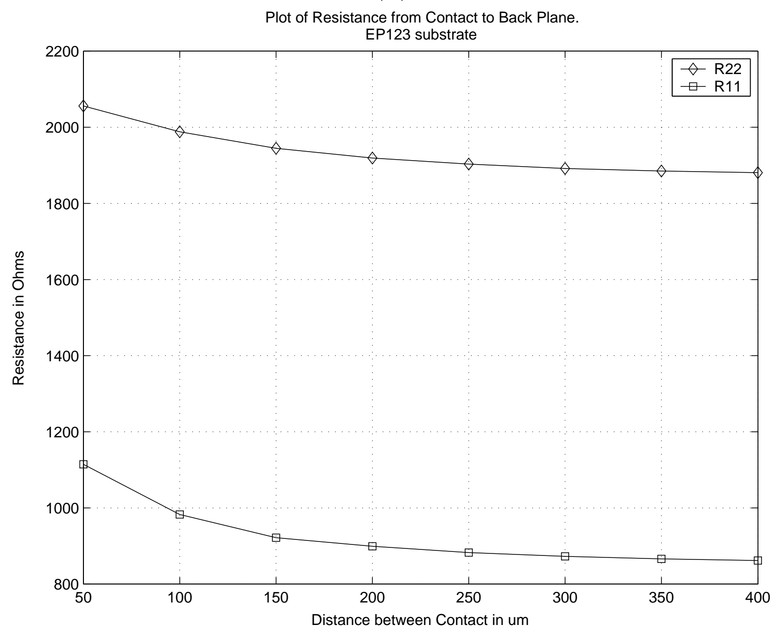


(b)

Figure 4.9: Plot of resistance (a) between contacts, (b) betweeb injector contact and back-plane, in a two contact analysis with Guard Ring surrounding the receiver contact in Subst-A.



(a)



(b)

Figure 4.10: Plot of resistance (a) between contacts (b) between Injector contact and back-plane, in a two contact analysis with Guard Ring surrounding the receiver contact in Subst-B.

package. Having multiple Guard Ring around various contacts will be beneficial for this substrate as every additional Guard Ring can eventually multiply the resistance between the contacts of interest and therefore isolation. However, in general analog IC design, Guard rings consume area and also great care must be taken while considering grounding of the Guard Ring as negligence may create a low resistance path between the contacts through the Guard Ring. However, substrate taps which are less area consuming are used in various points on the substrate too to sink in substrate currents.

In the case of Subst-B, from the plots in Figure 4.10, the effective impedance between the injector and receiver contact is almost unchanged even in the presence of a Guard Ring. The effective impedance increases rapidly with distance between contacts which is similar to the case without Guard Ring. Hence the effect of adding a Guard Ring on isolation cannot be expected in this case. As discussed, it is because of the fact that there is significant current flow in the bulk than through the surface. This is also highlighted by the plot of resistance to back-plane where the resistance almost stays constant as the separation between the contacts increases beyond a certain limit. Rather than using Guard Rings for this case, at the circuit level, this current flow through the bulk can be prevented by devising a proper grounding scheme for the back plane. We can get a better understanding of this when we look at the plots from circuit level simulations in the following section. Thus, we can conclude that the benefit of Guard Ring in Subst-B is not very significant compared to improvements seen on Subst-A.

4.3 Isolation Analysis of Single-Ended Circuits

Having studied the resistance variations in the two substrates of interest in the previous section, we shall now consider the case of a circuit representation of coupling in the single-ended contact analysis consisting of two single ended circuits. Contact here refers to the active area of a transistor which is linked to the contact on the substrate through a coupling capacitor which, for example, may be a junction capacitor in a NMOS transistor. Understanding the substrate model was done with a p-type contact which is directly on the p-type substrate. Now for circuit analysis,

we consider a n-type S/D contact connecting the p-type contact on the epi through junction capacitors. Hence, the effect of junction capacitors, load and source resistance of injector and receiver will also be considered here. Following section gives a detailed analytical model of coupling between two single ended circuits.

4.3.1 Analytical Model for Coupling in Two Single-Ended Circuits

The isolation between contacts depends on several factors besides the substrate element model. These include the contact-to-substrate capacitance, the backplane to ground impedance, the frequency of operation and the load impedance connected to the injector and receiver contact. Before getting into the analytical model of coupling between circuits, let us understand how coupling is defined between circuits in terms of isolation/gain. We define isolation between contacts as the ratio of the voltage read at the receiver load to the voltage applied to the the injector node of the circuit. The equation form is given by,

$$\mathrm{Isolation(dB)} = -\mathrm{Gain(dB)} = 20\log\frac{\mathrm{V_{rcv}}}{\mathrm{V_{inj}}} \tag{4.3}$$

To understand how the substrate model can be incorporated at the circuit level to measure coupling, let us now consider a two sets of simple NMOS follower as an example. We have considered the following assumptions during the circuit level representation of the coupling model. First, the capacitance of all other components like metals is considered negligible compared to the junction capacitance of the NMOS transistors. The contact area now considered is based on combined area between the source and the drain of the follower transistor and the current source. Similarly, the receiver contact may be the combined source and drain area of another NMOS follower. The two NMOS followers are considered to be independent of each other. The effective coupling capacitance between the active area of the transistor to the contact in the substrate has been computed using the junction depletion capacitance

in units of $Farads/\mu m$. For the processes considered, the per unit N^+ depletion capacitance for the Subst-A process was 0.12 fF/μm^2. And the per unit N^+ depletion capacitance for the Subst-B process was 0.96 fF/μm^2. I assumed an effective area of $2500\mu m^2$ for the drain and source regions of the followers. This results in an effective depletion capacitance of 0.3pF and 0.24pF respectively for the transistors on Subst-A and Subst-B respectively. The reason for choosing these dimensions was also to compare the results of simulation with available results from publications to confirm the reliability of the tool. The load resistor is considered to be the load resistor at the output of the second NMOS follower. The load resistance is assumed to be a typical value of 50 Ω. Similarly, the source impedance is assumed to be the resistor at the source of the first NMOS follower. Hence the coupling signal is assumed to come from the circuit into the substrate. The back plane of the substrate is assumed to be inductively connected to ground. As also explained earlier, the substrate resistance model developed for the two contact problem can be considered to be the resistance network between two p-type contact on the substrate. Hence by adding the effective junction depletion capacitances, one can also take NMOS active areas in circuits into consideration. For the case of PMOS transistors, the n+ to p-substrate junction depletion capacitance of NMOS will be replaced by the n-well to p-substrate junction capacitance. The black-box connecting the two independent circuits will be the extracted substrate model that was presented in the previous sections. To understand the effect of the inductor and capacitor components on coupling we analyze the results at three frequencies, 100 MHz, 1 GHz and 5 GHz.

The resistance network of the substrate model and the additional circuitry discussed above for circuit analysis is shown in Figure 4.11. This schematic effectively gives a simple and complete representation of circuit level simulation of substrate coupling. The trends on coupling and in turn isolation is primarily controlled by the substrate model developed. However, additional circuit level analysis and techniques for designers to look at while optimizing for isolation in design is also considered here.

The value of every component in the schematic is either determined from the substrate resistance model or provided by the circuit designer. Hence the analytical

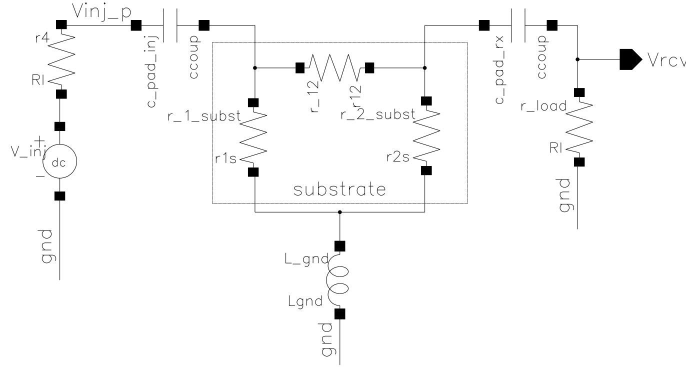


Figure 4.11: Schematic representation of the two contact single to single ended layout with injector and receiver circuitry.

formula for the measurement of isolation between two contact of any size and at any distance can be determined by measuring the ratio of the output voltage to the input. Changing the substrate resistance model in delta form to star form, the formula for isolation in terms of R, L and C parameters is,

$$V_{\text{out}} = \frac{\left(V_{\text{in}}\left(R_c + L_{\text{gnd}}\right) R_L\right)}{(C_i)(C_r)} \, . \tag{4.4}$$

where, $C_i = R_S + |\,(1/(2 * pi * f * C_c))\,| + R_a + R_c + L_{\text{gnd}}$ and

$C_r = R_L + |\,(1/(2 * pi * f * C_c))\,| + R_b$.

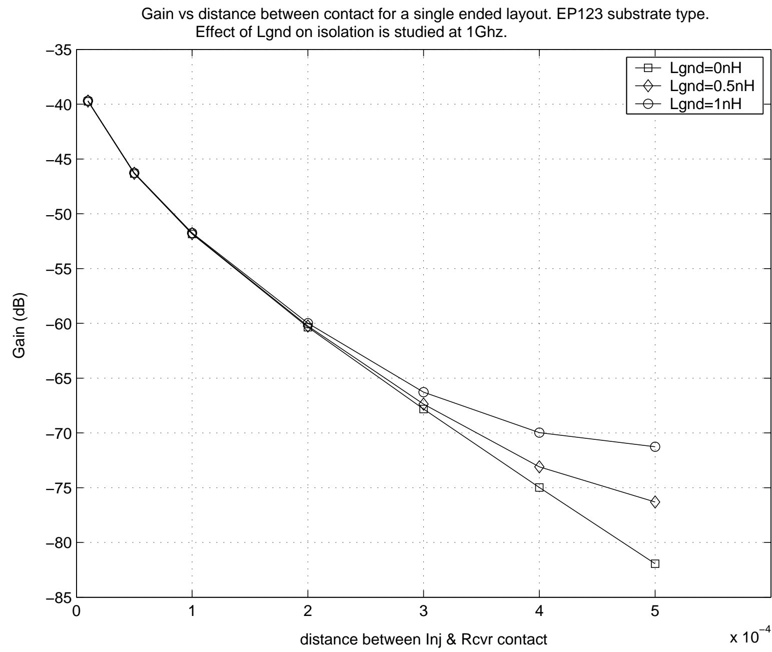
R_a, R_b and R_c are the equivalent star form representation of the substrate resistances R_{2subst} R_{1subst} and R_{12} in delta form. The parameters R_{2subst} and R_{1subst} can be determined using Figure 4.6(b) and similar family of curves based on varying contact dimensions for Subst-A and using Equation 4.2 for Subst-B. Parameter R_{12} can be determined using Figure 4.6(a) and similar family of curves for Subst-A and using Equation 4.1 for Subst-B. All other parameters can be provided by the designer to estimate the isolation. As can be deduced from the Equation 4.4, for better isolation, the source resistance R_S must be higher while the load resistor R_L need to be minimal. The junction to substrate depletion capacitance also need to be minimal which can be reduced by decreasing the size of the active area. However, the size of the transistor is also fixed by the requirements of the design. And as can be seen in the substrate resistance plots, decreasing the size of the active area increases the resistance in the resistance network between contacts. The isolation hence effectively increases. Back

plane impedance effect on isolation cannot be directly determined from formula. It depends on the resistance model of the substrate and we shall discuss it effects in the following section.

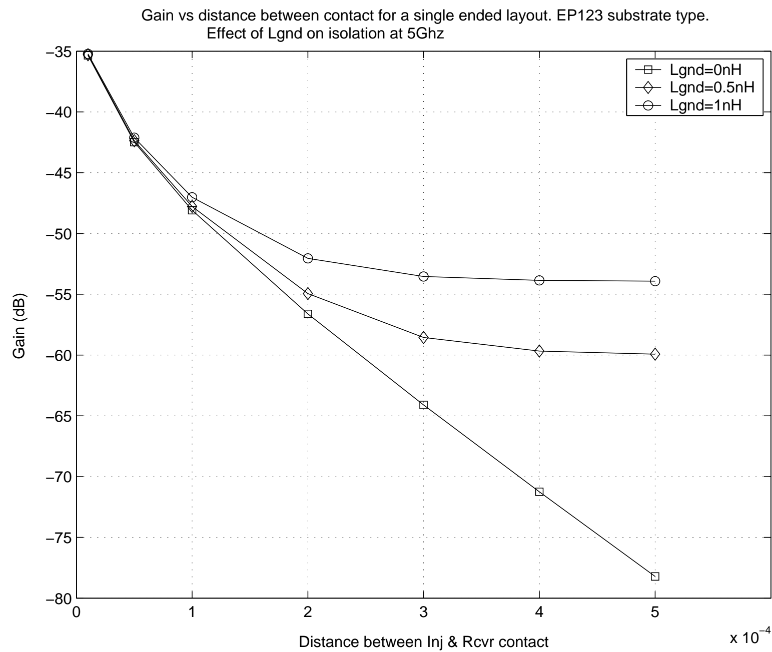
4.3.2 Effect of Back Plane Inductance on Isolation

As discussed in the analysis of substrate resistance models, the current sharing between the bulk and the epi and hence the resistance decide the need for proper back plane grounding schemes. Conclusions can be quickly drawn from plots on contact to back plane resistances that, in Subst-B, the flattening of the resistance plot after a certain critical distance will be a major concern while trying to improve isolation over distance. A proper back plane grounding scheme is the only better option to prevent the current flow through the bulk. As can be seen in Figure 4.12, the significance of better back plane grounding can be clearly seen. The plots are from simulation results done with substrate model extracted from Momentum. Result for the same analysis done using the Equation 4.4 is shown in Figure 4.13. The comparison between the computed gain and simulated gain at 5 GHz show close relation between the two. Exact match between them is not possible as there will be some difference between the substrate model extracted from simulations and substrate model created using curve fits and Equations 4.2 and 4.1. In perfectly low resistive substrates, where the bulk is heavily doped and epi are relatively thicker [1], the critical distance at which the current flow is completely through the bulk is approximately $5 - 10$ times the thickness of the epi-layer. This has been proved experimentally and published in [13].

A poor back plane grounding scheme with larger inductance hence has a significant degradation effect on the isolation as seen. A degradation of nearly 30 dB in isolation is seen when the back plane inductance is increased by 1 nH. Subst-A with resistance network in itself aiding significant current flow through the surface than through the bulk poses no major constraint on the kind of back plane grounding. A very poor grounding scheme will have only a very negligible effect on isolation in this case.



(a)



(b)

Figure 4.12: Plot of isolation (as Gain) versus distance between contacts in Subst-B for frequencies (a) f=100Mhz, (b) f=1GHz

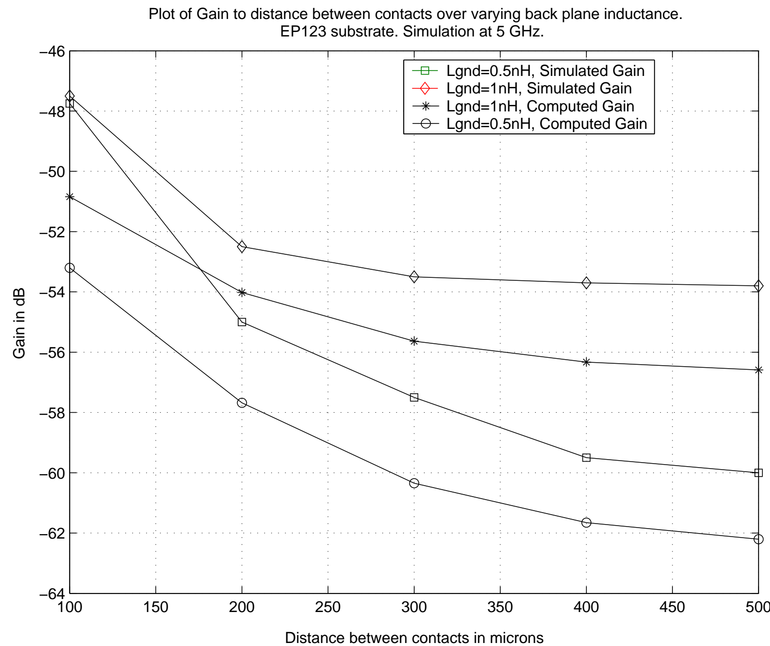


Figure 4.13: Plot of isolation (as Gain), computed and simulated versus distance between contacts in Subst-B at f=5 GHz.

4.3.3 Effect of Load and Source Impedance on Isolation

All simulations to study isolation in different layout topologies were done assuming a constant load of 50 ohms. However, the load impedance on-chip may be lower or higher. Since, the effect of load resistance on isolation is at the circuit level substrates will act similarly to load variations. Hence the analysis done on Subst-B will provide with similar results for both substrates. Assuming the substrate model parameters for a fixed distance between the contacts, the load impedance has been swept from 10 Ω ohms to 1 KΩ. The results of the analysis is plotted in Figure 4.14.

The load resistance value is generally chosen such that the capacitive reactance of the coupling capacitor is larger than the load in the frequency band of interest. The load impedance is the effective load looking into the device from the substrate. This definition of load includes the effective of the load including the effect of any feedback which may be present around the circuit. If the pole of the C-R is beyond the frequency of interest then the load will not affect the voltage division ratio between the substrate and the output.

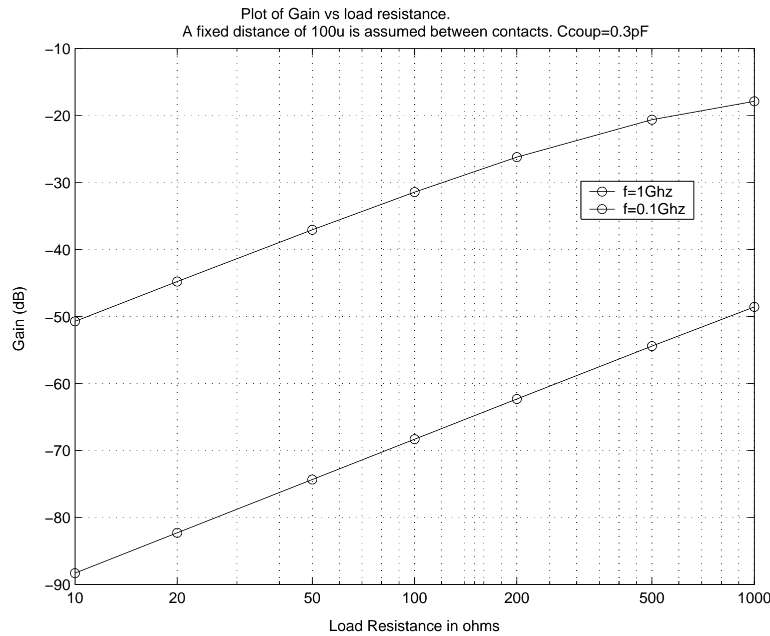


Figure 4.14: Plot of isolation (as Gain) vs load resistance for a single ended circuit topology.

Hence, for frequencies of operation lesser than the pole frequency for the maximum load, the output is just a voltage division of the substrate voltage at the receiver contact. In the current simulation, the pole frequency at the maximum load is approximately 500 MHz. Hence at an operating frequency of 0.1 GHz, with increasing load resistor, the isolation decreases linearly with the load resistance. For frequency of operation beyond the pole frequency, say, 1 GHz, there is a deviation from linearity in isolation for load resistances beyond 500 Ω. This is clearly seen in the plot of Figure 4.14. From Equation 4.4, we can conclude that if the load resistance is kept at a minimum in comparison to the coupling capacitor into the substrate, the overall isolation can be kept at a maximum. To avoid any deviation in expected isolation, it becomes mandatory to have the pole of the C-R at a frequency beyond the frequency of interest.

Let us consider a transmission line example as shown in Figure 4.15. The transmission line is assumed such that the differential transmission line do not have a balanced coupling with the differential lines connecting the receiver. With the in-

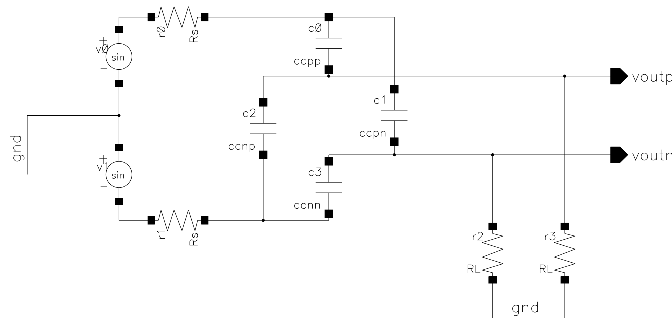


Figure 4.15: Transmission line analysis to understand the effect of impedances on isolation.

herent imbalanced isolation provided by the different coupling capacitors that are coupling the two differential lines, the only other factor under the control of the designer is the source and load impedances connected to the lines. As can be expected from the analysis above, the effective isolation can be improved by having a bigger source resistance and a smaller load resistance. This will effectively put the R-C pole below the frequency of interest and the C-R pole above the frequency of interest for a given coupling capacitance.

4.3.4 Effect of Guard Ring on Isolation

As we have already discussed on how the resistance plots change with the addition of guard rings to the substrates earlier in the chapter, let us just analyze the requirements for better isolation using Guard Rings from the point of view of a designer.

We have seen that the effect of adding a Guard Ring has significance in Subst-A. That is because, the model of the substrate aids significant current flow on the surface. The addition of a P+ Guard Ring creates a shorter resistance path to it from the injector contact. This effectively isolates the receiver contact from the injector by increasing the resistance between them by more than 10 times for the sizing we considered. Since the effective resistance in the substrate model change significantly with and without Guard Rings, in Subst-A, the effect of guard ring grounding schemes also will be significant in Subst-A to achieve good isolation. Subst-B as seen earlier had no major substrate resistance changes with the addition of Guard Rings and hence

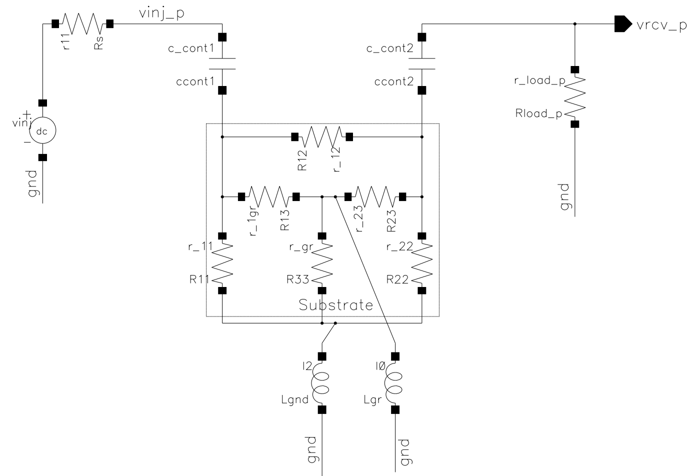
no significant improvement in isolation expected.

We can immediately conclude that the addition of many substrate taps and guard rings in Subst-A, will reduce coupling significantly. Since the purpose of the Guard Ring is to provide the least resistance path to ground from the substrate, the Guard Rings are typically shorted to ground using a bond-wire. The issue for the designer however is the methodology to be followed while grounding the guard ring to further improve isolation.

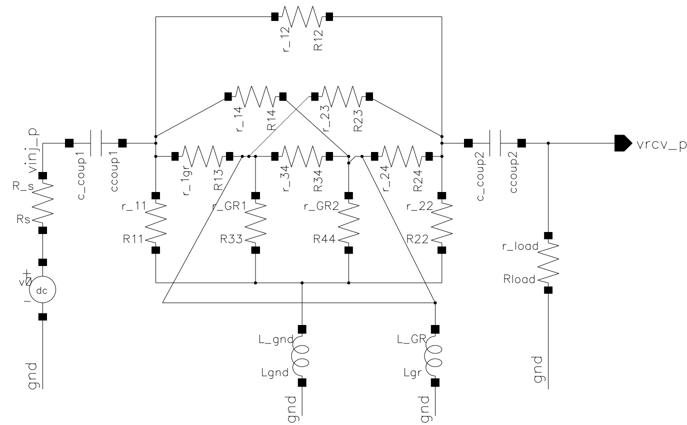
The schematic of a two contact substrate model is now changed to a three contact problem with the addition of guard ring. The corresponding resistor model translates to a four resistance network as shown in Figure 4.16(a). The schematic also shows the bond wire (L_{gr}) connecting the Guard Ring contact(3) and the ground plane. The plots to be shown here discusses the effect of inductance associated with Guard Ring bond wires to ground on isolation. The effect of grounding multiple guard ring through a common bond wire will be seen later.

Bond wires are small inductors carrying a certain inductance in them. Hence in high frequency circuits, this inductance will provide a significant resistance in the bond wires. As can be seen in the plot of Figure 4.17, the effective isolation slowly decreases with increasing Guard Ring inductance.

This may not be a major concern when having a single guard ring in the circuit of interest where this variation is inevitable. Let us suppose, the designer decides to have an additional Guard Ring around the injector too. We are considering Subst-A for this analysis. This will further improve the isolation as expected by an additional 15 dB just from the substrate resistance model. The equivalent schematic of the circuit with the substrate resistor model is shown in Figure 4.16(b). Let us assume a case where the designer decides to use a common bond wire connecting the two guard ring contacts to ground. If in this case, for the package of interest, the bond wire inductance in the package used is significant and unexpected higher, the designer has himself inadvertently created a good short circuit between the guard rings. If we assume the physical distance between the contacts as 100 μm and the guard rings approximately 10 μm away to each of the contacts, the effect of having a common bond wire with higher inductance to both the Guard Rings can cause a physical short



(a)



(b)

Figure 4.16: Schematic representation of the two contact single to single ended layout with: (a) Guard ring circuitry around the Receiver, (b) Guard ring circuitry around both Injector and Receiver.

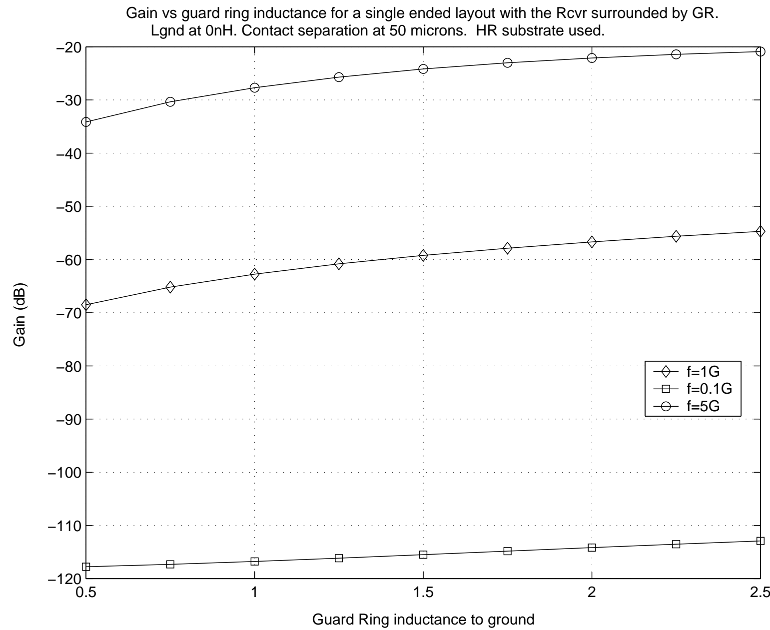


Figure 4.17: Plot of isolation (as Gain) vs Guard Ring inductance to ground in Subst-A with guard ring surrounding the Receiver.

between the guard rings and can cause the contacts that is physically 100 μm away to be as close as 40 μm. The effective resistance between the contacts will hence be, the resistance between the contact and its guard ring and the resistance of the metal shorting the two guard rings to a common bond wire connection. The isolation related to that distance. This is confirmed by the plot of Figure 4.18. Hence, in cases where isolation is necessary and area not a concern, it is mandatory to have individual bond wires to ground from circuits that require sufficient isolation. A similar case, see Figure 4.19, for Subst-B shows no significant change in isolation as expected and hence the need to have separate bond wires to ground from the guard ring is hence not mandatory.

4.4 Isolation Analysis of Fully Differential Circuits

The second topology under coupling analysis is the fully differential circuits. In a circuit design point of view, fully differential circuits have significant advantages

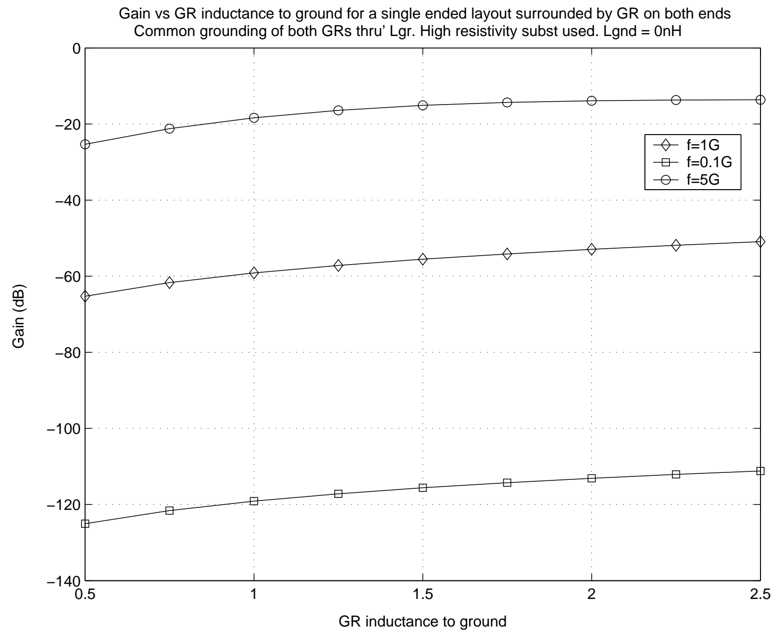


Figure 4.18: Plot of isolation (as Gain) vs Guard Ring inductance to ground in Subst-A with common grounding of Guard Rings.

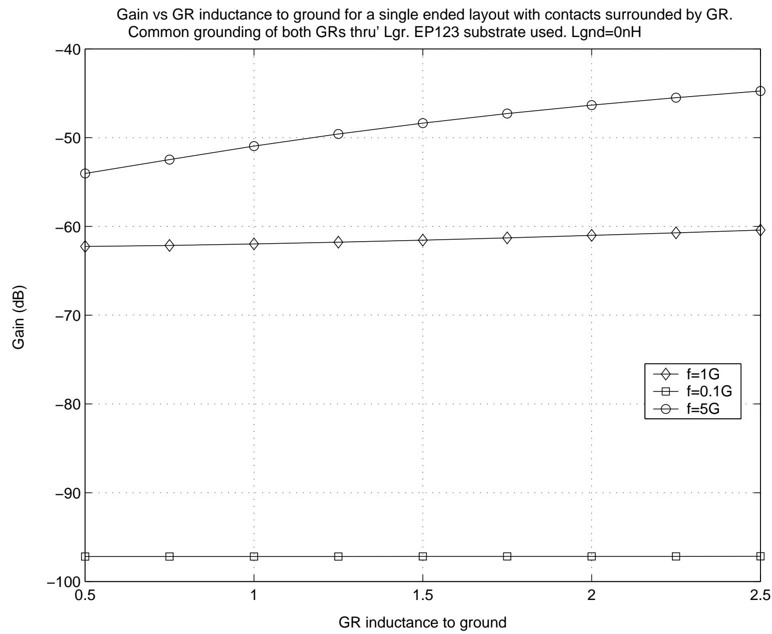


Figure 4.19: Plot of isolation (as Gain) vs Guard Ring inductance to ground in Subst-B with common grounding of Guard Rings.

on noise reduction when it is in a balanced mode. To look at the advantages of a fully differential layout model on substrate noise coupling, let us use the substrate resistance results for a two contact model and develop an equivalent model for the differential structure.

We consider the differential structure to be two fully differential circuit topologies which are independent of each other at the circuit level. We connect the two structures together through the substrate resistance model, that exist between the contacts that the active layers form on the substrate. Although, two transistors of a differential pair have relation between them in the circuit sense, in a substrate, they can be considered as two independent contacts. We, relate them by injecting noise signals whose magnitudes are complement to each other for differential analysis.

4.4.1 Analytical Model for Coupling in Differential Topology

As we have already made a detailed analysis of the substrate resistance model for a two contact problem, we are approaching the differential 4 contact model as multiple two contact models for simplicity of analysis and to use the available resistance plots and equations for resistance to back plane and between contacts.

The layout of 4 contact differential layout problem is shown in Figure 4.20. The complex resistance model of the substrate involving the four contacts is shown in Figure 4.21. The schematic also includes the junction capacitors connecting the active area of the drain and source of the transistors and also the corresponding source and load resistors of the differential injector and receiver.

For analytical purposes, the complex substrate resistivity model is broken such that circuit analysis for coupling is done between only two contacts at a time, an injector and a receiver contact. Using their contact distance and sizing information, the corresponding resistance value between contacts and contact to back plane for Subst-A and Subst-B are determined. The values can be taken by either looking at the family of curves similar to as in Figures 4.6 and 4.7 for the corresponding sizing and contact area or using the formulas developed for Subst-B as shown in Equations

Figure 4.20: Layout of a fully differential contact problem.

Figure 4.21: Schematic representation of the fully differential ended structure with injector and receiver circuitry.

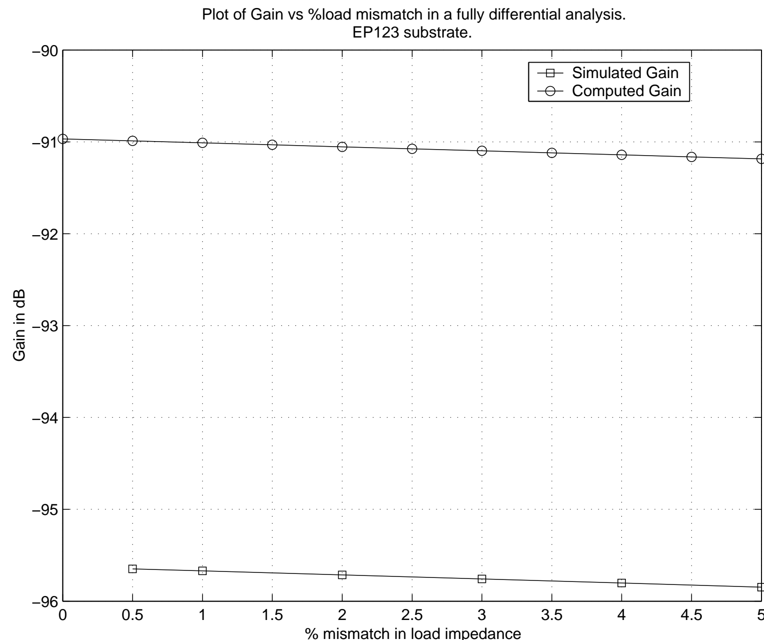


Figure 4.22: Plot of simulated isolation (as gain) and computed isolation (as gain) for a differential layout over mismatch in load resistance.

4.2 and 4.1. Using the value of substrate resistances, junction capacitance, load and back plane inductance, the voltage coupled into the receiver contact from the injector can be determined using Equation 4.4. This process is similarly repeated for all other contact pairs between the injector and the receiver. Overall, we will have four values of voltage coupled from the two injectors into the two receivers. In this case in Figure 4.20, we will have voltage coupled from contacts 1 to 2, 1 to 3, 4 to 2 and 4 to 3 respectively. The coupled voltages converging to the two receivers are summed and the differential voltage between them determined. From this the effective isolation is determined using Equation 4.3. This analytical methodology has been followed for Subst-B to compute the effective isolation for a balanced differential ended contact structure with load resistance mismatch at 100 MHz. The result is shown in Figure 4.22. The mismatch between the results in comparison to the simulated value in Figure 4.25 was less than 5 dB. This difference can be expected as the effective coupling between the injectors itself is not considered for simplicity sake. Also the simulated substrate resistance and computed substrate resistance values cannot exactly match.

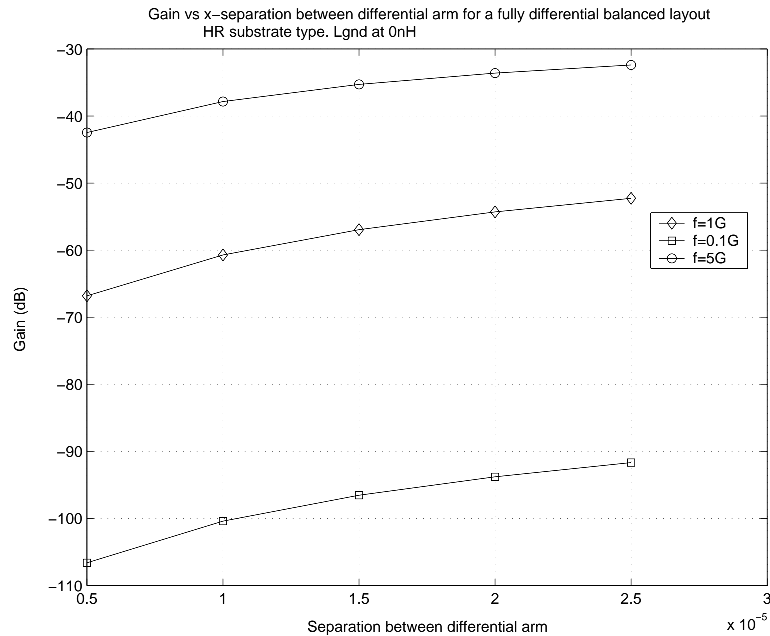


Figure 4.23: Plot of isolation (as Gain) versus separation between the differential arms of a full differential contact in Subst-A.

This may be due to the fact that computed substrate resistances are from plots of two contact analysis while the simulated substrate resistances are from the simulation of four contact analysis. However, the error due to them is not very significant.

Having developed a analytical model and checked for closeness to simulated result, we digress and follow up with discussion of advantages of differential layout on isolation and its immunity to component mismatches on isolation.

4.4.2 Effect of Differential Arm Separation on Isolation

The first analysis done was to see how the layout in itself affect isolation when the differential arms are separated about the Y-axis. Using the structure in Figure 4.20 the separation between the differential arm of injector and receiver contacts were increased and the corresponding resistance variation in the substrate were recorded from simulation. The extracted model was used in a circuit simulator to measure isolation. The results from the analysis is shown in Figure 4.23 and 4.24. With increase in X-separation between the contacts along the X-direction, we see a gradual

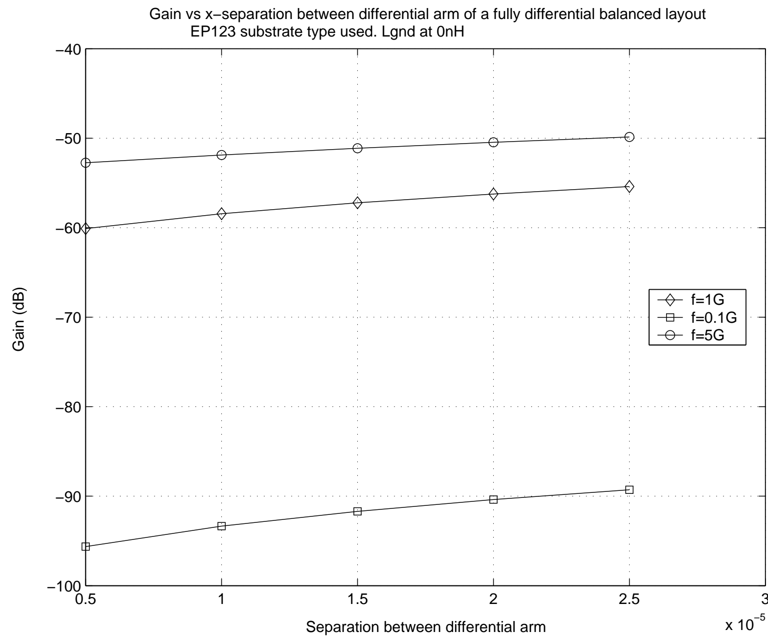


Figure 4.24: Plot of isolation (as Gain) versus separation between the differential arms of a full differential contact in Subst-B.

decrease in effective isolation. This reason can be explained as follows. As the x-separation between contacts increases, the diagonal resistance between contact ports 1-2 and ports 3-4 increases. However, the resistance between the injector and receiver contact in the vertical direction remain the same. This effectively reduces the cancellation effect between the injector signals from contact 1 and 4 which are complement to each other. Hence the effective signal at the receiver contact increases and also the coupling. Thus, the more closely spaced the contacts are, the better will be the isolation for the same Y-separation between the injector and receiver contacts. The trend is similar in both substrates as seen in the plots. The effect is more significant in Subst-A as most of the injected current flows through the surface through the vertical and diagonal resistances between contacts. A similar trend in isolation is also seen in Subst-B but with a lesser effect.

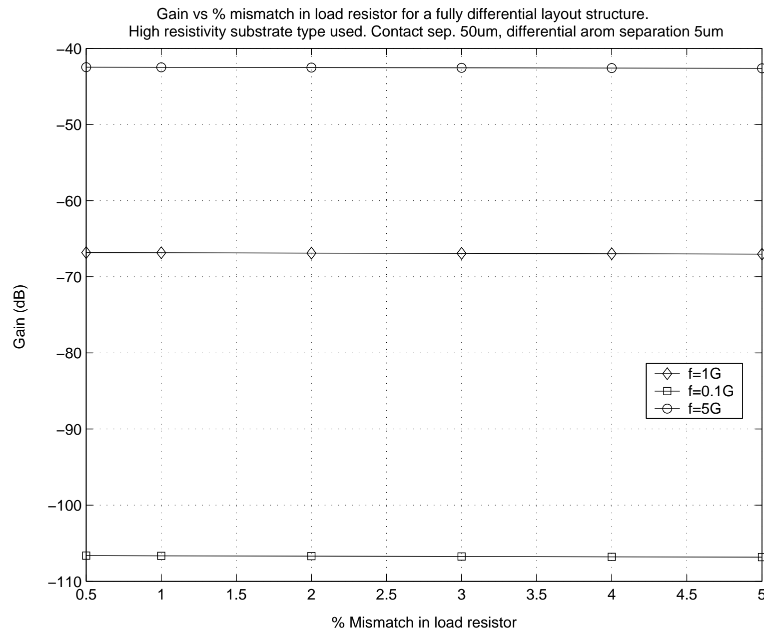


Figure 4.25: Plot of isolation (as Gain) versus percentage load mismatch between the differential load resistors in Subst-A.

4.4.3 Effect of Load Mismatch on Isolation

Let us now consider the analysis of load mismatches on isolation in a fully differential contact layout. A balanced layout is assumed and only load mismatch at the circuit level introduced. The simulation uses the same layout structure with the Y-separation between injector and receiver fixed at 50 μm and an X-separation between the differential contacts at 5 μm to have proper differential behavior. Simulation results of isolation versus percentage mismatch between load resistances is shown in Figure 4.25 and Figure 4.26 for Subst-A and Subst-B respectively.

The plots show that the isolation between the injector and the receiver has very minimal impact caused by the mismatched load resistance. Even for a higher percentage variation between the load resistances, the effective isolation changed by less than a dB as shown in Figure 4.27. The advantage of a fully differential structure is seen in this analysis. The reason for the immunity to load mismatches is that, the substrate resistance network between the contacts are symmetric when the layout structure of the differential injectors and receivers are balanced and the contacts at

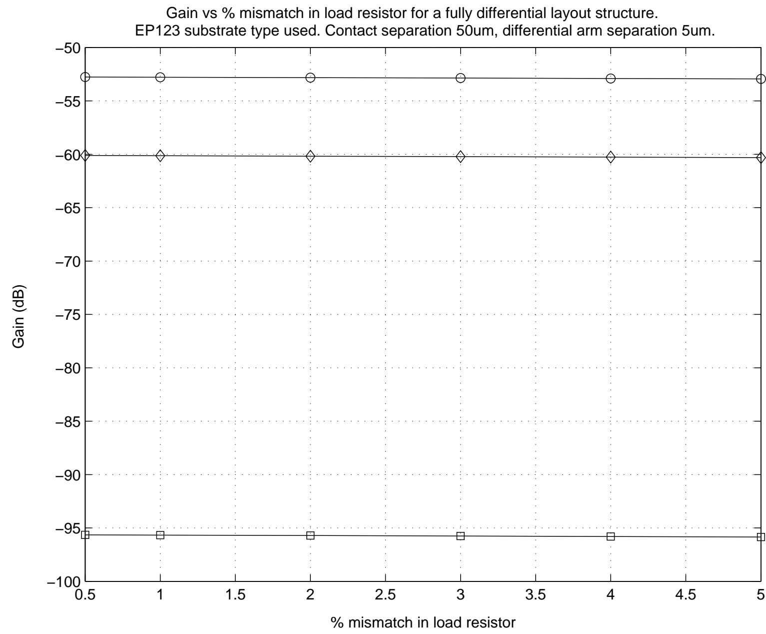


Figure 4.26: Plot of isolation (as Gain) versus percentage load mismatch between the differential load resistors in Subst-B.

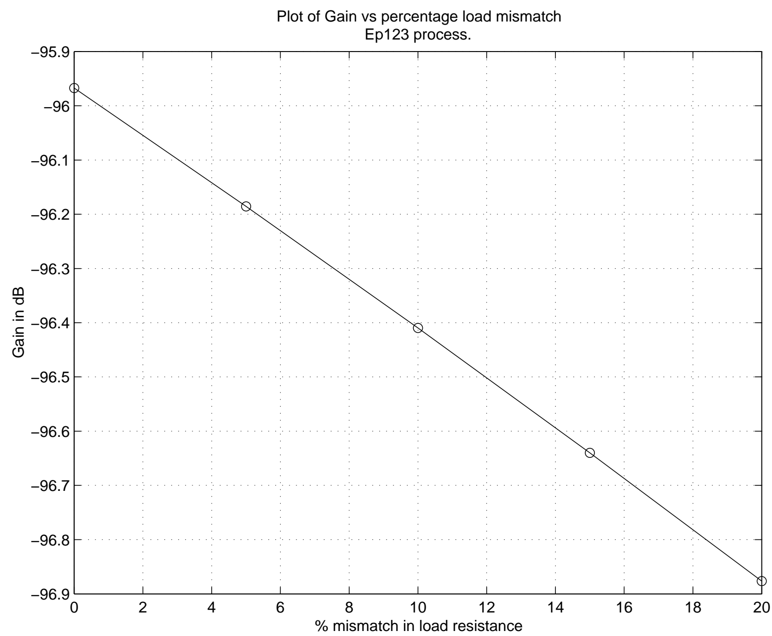


Figure 4.27: Plot of isolation (as Gain) versus percentage load mismatch between the differential load resistors in Subst-B.

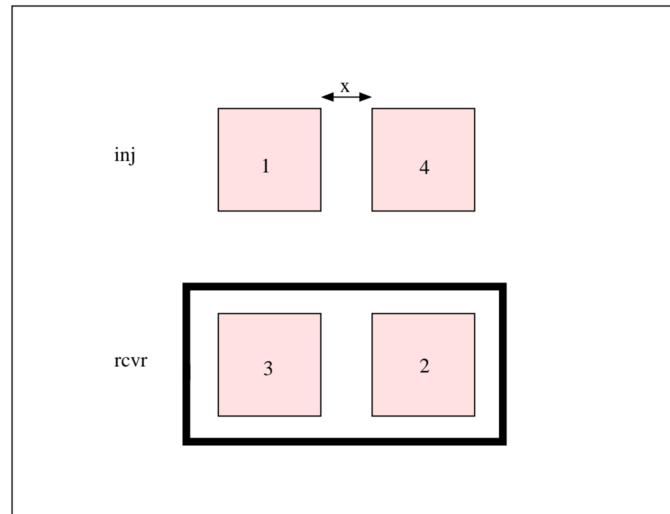


Figure 4.28: Layout of a fully differential contact problem with guard rings surrounding the receiver.

each end closely placed. The cross-coupled symmetric nature leads to proper distribution of coupling currents between the injector and the receiver irrespective of the mismatches in the load resistors. Hence the effect of load mismatch at the receiver end contact is nullified significantly. This advantage is due to the balanced nature of the structure and hence the effect is seen equally in both substrate types as shown in the plots.

4.4.4 Effect of Guard Ring on Isolation

The effect of Guard Ring on substrates have been discussed in the single ended contact structures in the earlier sections. The manner in which the resistance distribution varies based on the substrate type have also been discussed in detail. Going on similar lines an analysis of Guard Ring addition to differential structure is studied. The layout of the differential contact with Guard Ring surrounding the receiver is shown in Figure 4.28 and the resulting substrate resistance network with circuit level components is shown in Figure 4.29.

Circuit analysis to understand the effect of Guard Ring is done on for the case of isolation for x-separation between contacts. This was done to compare results with

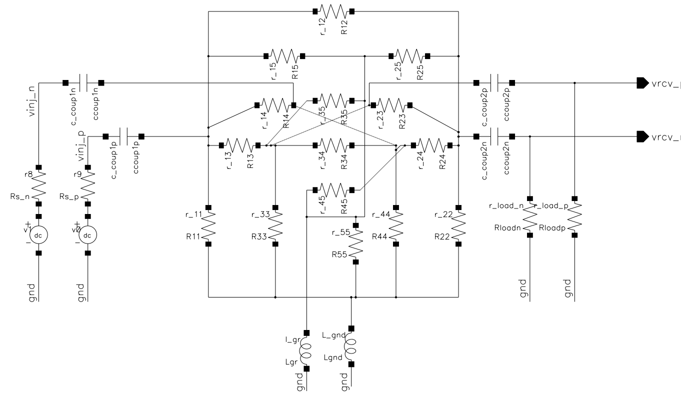


Figure 4.29: Schematic representation of the fully differential ended structure with additional guard ring circuitry.

and without Guard Ring. Simulation results are shown in Figure 4.30 and Figure 4.31 for Subst-A and Subst-B respectively.

As in expected lines, the effective floor of isolation has improved by approximately 50 dB in Subst-A. Subst-B has can be expected has no significant impact. The variation in isolation over separation between the differential arm remains unchanged as with the case without Guard Ring. Though the guard ring sinks in significant amount of surface current from the injector, the effective ratio of the vertical and diagonal resistance between the injector and receiver contacts remain the same. This ratio is what decides the effective cancellation. Since Guard Rings don't cater this effect, we see the same trend in isolation to x-separation between contacts.

4.5 Summary

This chapter deals with the core of the research work done for this thesis. The first part of the research dealt with understanding substrate models. Two substrates types were considered. Resistance model for the substrate for a single contact and two contact structures were developed. Plots of substrate resistance over contact size and contact spacing were developed for the substrates. Analyzing the plots helped in understanding the effective behavior of the substrate. Conclusions were drawn on the distribution of substrate current flow in the substrates. From the plots of substrate

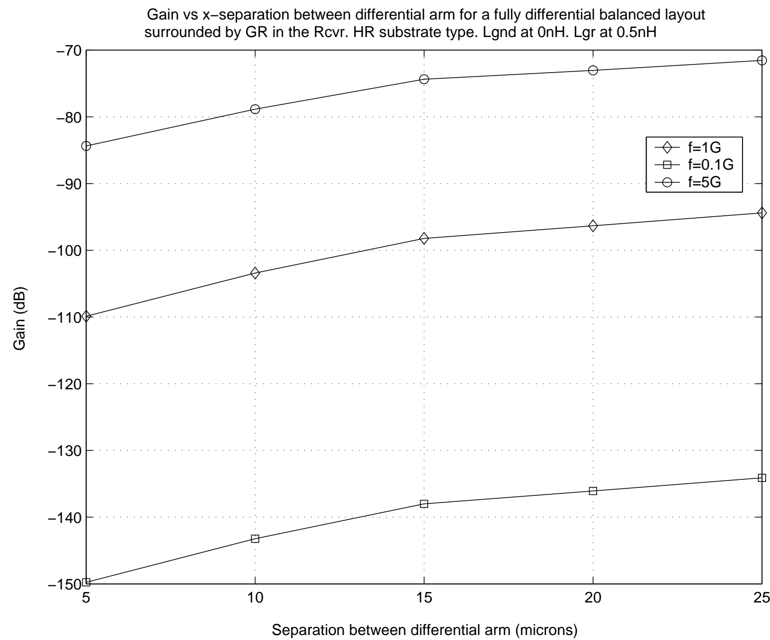


Figure 4.30: Plot of isolation (as Gain) versus separation between the differential arms of a full differential contact in Subst-A with guard rings surrounding the receiver contacts.

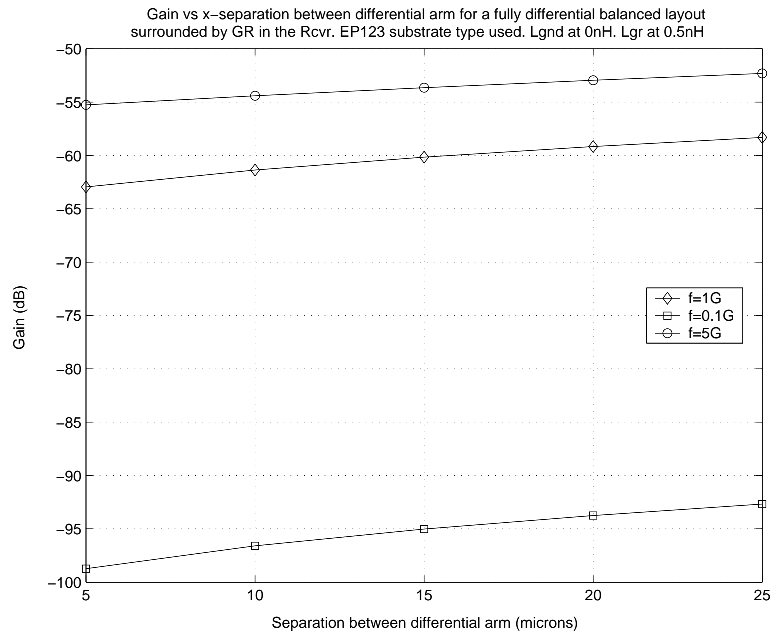


Figure 4.31: Plot of isolation (as Gain) versus separation between the differential arms of a full differential contact in Subst-B with guard rings surrounding the receiver contacts.

resistance in Subst-B, it was found that current flow is effectively only through the bulk after a certain critical distance. An effective formula for developing the plot of substrate resistance for Subst-B was developed. The equation was effectively used to rebuild plots for different contact spacing with some fitting parameters extracted from simulated plots. Guard Ring effect on substrate resistance model was studied. The effectiveness of Guard Ring on Substrate was understood in Subst-A, where the redistribution of resistances on the surface caused significant isolation improvements.

Following the analysis of the substrate, circuit level analysis of substrate coupling was analyzed. A simple circuit model has been developed and its connection to the substrate has been discussed. The resistance model of the substrate was used in the circuit analysis to understand the interaction between the independent circuits. A close form equation for computing isolation between the injector and receiver, based on the circuit parameters and substrate resistance model was developed. The circuit level analytical model was used to generate plot to compare the results from simulations. Further, analysis was done to understand how certain circuit level parameters like back plane inductance, guard ring inductance, bond wire connections to ground, load resistance, etc., affect isolation and techniques to improve isolation using these parameters have been proposed.

Finally isolation analysis on Differential contact layout have been studied. Using the already developed plots and equation for a two contact model, the results have been extended and used in the analytical analysis of the differential contact problem. The four contact differential model was simplified into multiple set of two contacts and circuit analysis using the equation developed for two contact analysis were used. At any time, coupling between a injector and a receiver contact was computed. The final results were combined to generate the result for a four contact differential model. This approach followed for simplicity gave isolation results that closely matched the results from circuit simulations. Further, simulation were done and plots were generated to understand how different factors like spacing in differential layouts, Guard Ring, load imbalances affect isolation and also how differential layout model handle these variations in itself.

Chapter 5

Conclusions and Future Work

Substrate coupling in integrated circuit is one of the major design concern in research over the past few years. Different experiments have been approached by researchers to get a better understanding of the substrate and its effects on the circuits built over it.

The current thesis presents a simple methodology for designers to predict isolation in circuits. The accuracy comes from using an accurate resistance model of the substrate. This is clear as the substrate plays a significant role on coupling between circuits in a chip. Hence a detailed analysis to understand the substrate resistance model was carried out. The variation of substrate resistance between contacts and between contact and backplane was studied and trends of each in different substrate types were studied. As part of the study on the substrate resistance model, the effect of a Guard Ring built on the substrates was studied. The distribution of resistances based on the addition of a Guard Ring on different substrates, helps in understanding how Guard Ring improves isolation in different substrates. A equation form to compute substrate resistance model was developed based on contact sizing and spacing for Subst-B. The equation developed and plots from simulations of the substrate resistance model were used in determining an analytical equation to compute isolation between two contacts on a substrate. The coupling part of realistic circuits modeled as parasitic components were used to develop the equation for computing coupling between circuits. The analytical model of coupling in single ended topology was

applied to compute coupling in differential circuit topologies. Simple and realistic assumptions have been taken while computing coupling in differential topologies. The analytical models have been proved for correctness by comparing the computation results with simulations for the same conditions.

As a second part of the thesis, circuit component effects on isolation in single and differential ended circuit topologies were analyzed. Circuit parameters useful for improving coupling were varied to study how they improve or affect isolation in circuits on different substrates. From the analysis, specific design ideas to improve isolation on different circuit topologies on substrates of interest have been presented.

As directions to future work in this area, instead of having a family of substrate resistance plots for circuit level isolation analysis, an efficient formula based computation of substrate resistance model can be determined. A closed form solution for this purpose based on the substrate properties, contact sizing and area could be developed for all substrate types. A example model has been shown for Subst-B in this thesis. A similar model for all substrates would be very useful for simple analysis. The modeling can be done by having a general $N \times N$ matrix formulation of Z or Y parameters relating the N contacts on the substrate. The result can then be extended to other complex cases of irregular shapes of contacts without losing any vital information necessary for accurate substrate resistance modeling and isolation prediction in circuits.

Bibliography

[1] R. Gharpurey and R.G. Meyer, “Modeling and Analysis of Substrate Coupling in Integrated Circuits,” *IEEE Journal of Solid-State Circuits*, Vol. 31, pp. 344-353, March 1996.

[2] T. Smedes, “Extraction of Circuit Models for Substrate Cross-talk,” *Proc. of the International Conf. on Computer Aided Design*, pp. 199-206, November 1995.

[3] , A.J. Van Gendersen, “http://www.space.tudelft.nl/”.

[4] N.K. Verghese, “Verification of RF and Mixed-Signal Integrated Circuits for Substrate Coupling Effects,” *IEEE Custom Integrated Circuits Conference*, pp. 363-370, May 1997.

[5] N.K. Verghese, “SUBTRACT: A Program for the Efficient Evaluation of Substrate Parasitics in Integrated Circuits,” *Proc. of the International Conf. on Computer Aided Design*, pp. 194-198, November 1995.

[6] E. Charbon, “Substrate Optimization Based on Semi-Analytical Techniques,” *IEEE Transaction on Computer-aided design of Integrated Circuits and Systems*, Vol. 18, pp. 172-190, February 1999.

[7] E. Charbon, “Substrate Noise: Analysis and Optimization for IC design,” *Kluwer Academic Publishers*, 2001.

[8] R.G Meyer, “Analysis and Design of Analog Integrated Circuits,” *Wiley Publications*, 4 th Edition, April 2002.

[9] D. Ozis, "An Efficient Modeling Approach for SUbstrate Noise Coupling Analysis," *International Symposium on Circuits and Systems* , May 2002.

[10] R. Gharpurey, "A Methodology for Measurement and Characteristic of Substrate Noise in High Frequency Circuits," *IEEE Custom Integrated Circuits Conference*, pp. 487-490, May 1999.

[11] M. Hasegawa, "Properties of microstrip lines on Si-SiO_2 systems," *IEEE Transaction on Microwave Theory and Techniques*, vol. 19, pp. 869-881, November 1971.

[12] A. Samavedam, "A Scalable Substrate Noise Coupling Model for Design of Mixed-Signal IC's," *IEEE Journal of Solid-State Circuits*, pp. 895-904, June 2000.

[13] D.K. Su, "Experimental Results and Modeling Technique for Substrate Noise in Mixed-Signal Integrated Circuits,", *IEEE Journal of Solid State Circuits*, pp. 420-430, April 1993.

[14] "Agilent EEsof Momentum, Electromagnetic Design and Simulation, Advanced Design System 1.5," *Agilent Technologies*, December 2000.